

# Compal Confidential

## VBA20 LA9303P Schematics Document

INTEL SandyBridge C847/C807 CPU with DDRIII + PCH NM70

AIO M/B

UMA only

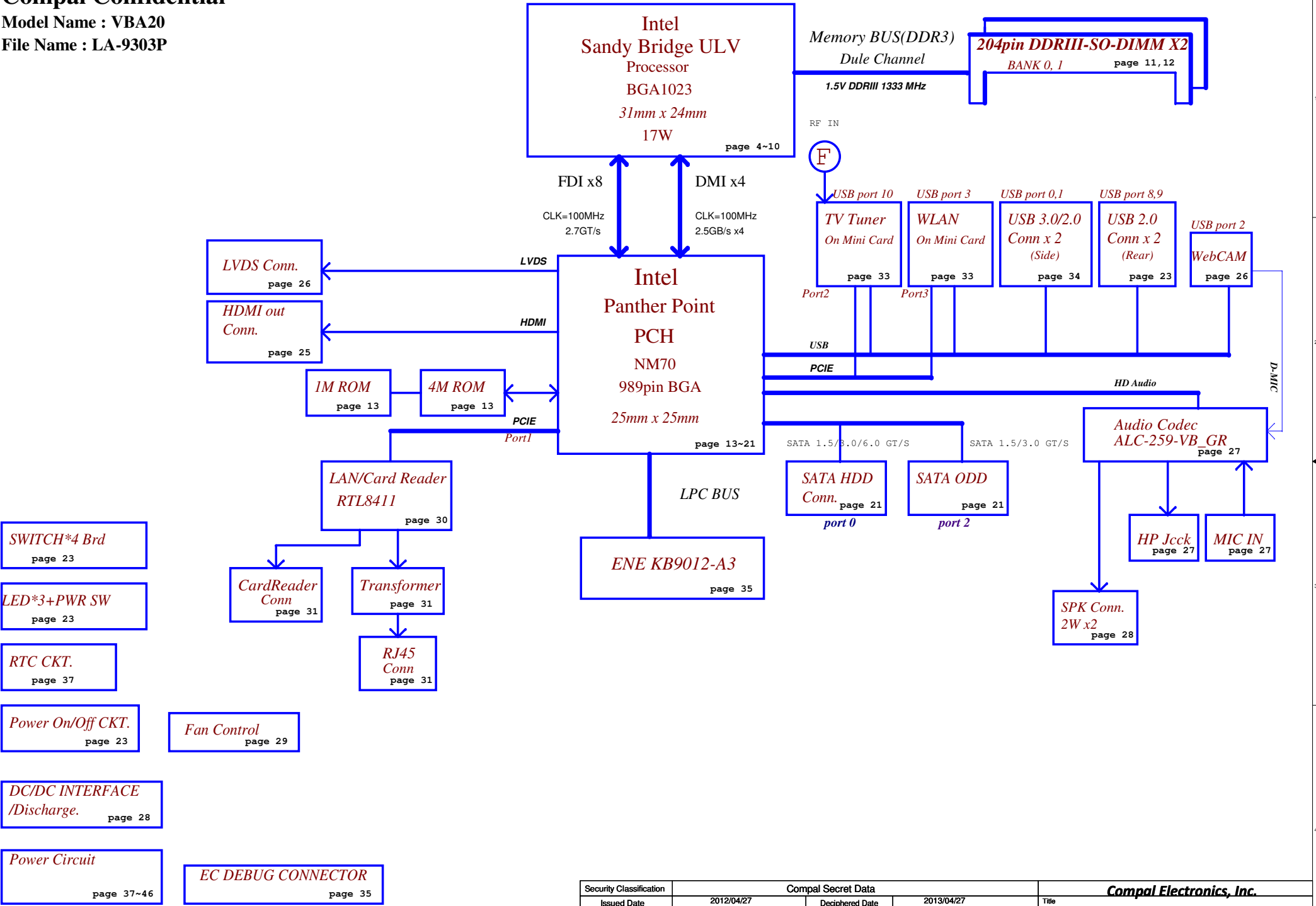
REV: 0.1

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Model Name : VBA20

File Name : LA-9303P



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+VCCSUS3_3	+3VALW to +VCCSUS3_3 power rail for PCH	ON	ON	ON*
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTT power rail for CPU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

<i>STATE</i>	<i>SIGNAL</i>	<i>SLP_S1#</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>
Full ON	HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF

## EC SM Bus1 address

## EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
--------	---------	-----	--------	---------	-----

## SM Bus Controller 0

Device	Address	HEX
--------	---------	-----

## SM Bus Controller 1

Device	Address	HEX
--------	---------	-----

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
R2672	0			
Board ID	Rb / Rd / Rf	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	0 V	0 V	0 V

## PCIE(GPP) Port Table

Port	Device
1	LAN/Card reader
2	Mini Card(TV Tuner)
3	Mini Card(WLAN)

## SATA Port Table

Port	Device
6G	0 HDD
	1 Disabled on NM70
3G	2 ODD
	3 Disabled on NM70
	4 NC
	5 NC

## USB Port Table

USB 2.0	USB 1.1	Port	Device
EHCI	OHCI	0	USB (side I/O)
		1	USB (side I/O)
		2	Web Camera
		3	Mini Card(WLAN)
		4	Disabled on NM70
		5	Disabled on NM70
		6	Disabled on NM70
		7	Disabled on NM70
EHCI	OHCI	8	USB20- (Rear I/O)
		9	USB20 (Rear I/O)
		10	Mini Card(TV Tuner)
		11	NC
		12	Disabled on NM70
		13	Disabled on NM70

## BOM Structure Table

BTO Item	BOM Structure
CPU C807	807@
CPU C847	847@
PCH NM70	NM70@
PCH HM70	HM70@
ME components	CONN@
Unpop	@
USB30	USB30@
LA-9303P 6 Layer PCB	
SKU IO Select	GPIO64_H@
	GPIO64_L@
	GPIO65_H@
	GPIO65_L@
PANEL Select	ID0L@
	ID0H@
	ID1L@
	ID1H@

## SKU ID(Project) Table

Project_ID2 (GPIO189)	Project_ID1 (GPIO190)	SKU	
0	0	SKU1	807@ NM70@ ID0L@ ID1L@ GPIO64_L@ GPIO65_L@
0	1	SKU2	847@ NM70@ ID0L@ ID1L@ GPIO64_H@ GPIO65_L@
1	0	X	
1	1	X	

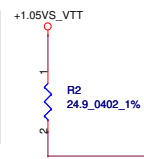
## BOARD ID Table

Board ID	PCB Revision
0	0.1
* 1	0.2
2	0.3
3	0.4
4	

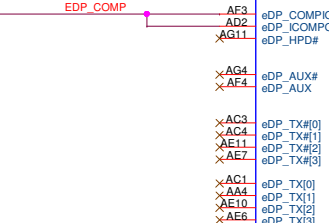
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eDP\_COMP0 and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms, even if disable eDP function...



W=12mil L=500mil S=15mil



IVYBRIDGE\_BGA1023  
C867@

PCI EXPRESS -- GRAPHICS

W=12mil L=500mil S=15mil



C867@ Celeron 867 HR 1.3G SA00005BH40(S IC AV8062701148901 SR0FK J1 1.3G ABOI)

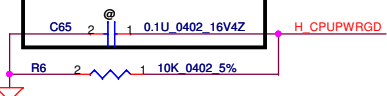
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

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								PROCESSOR(1/7) DMI,FDI,PEG			
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PCH->CPU  
UNCOREPWROK:非CORE外的電OK  
SM\_DRAMPWROK:DRAM power ok  
RESET#:都ok後請CPU做reset

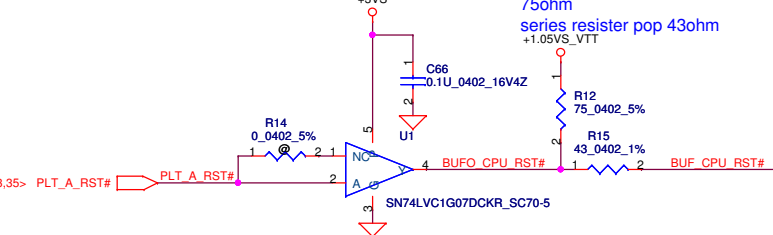
Follow DG 1.5& Tacoma\_Fall2 1.0

reserve



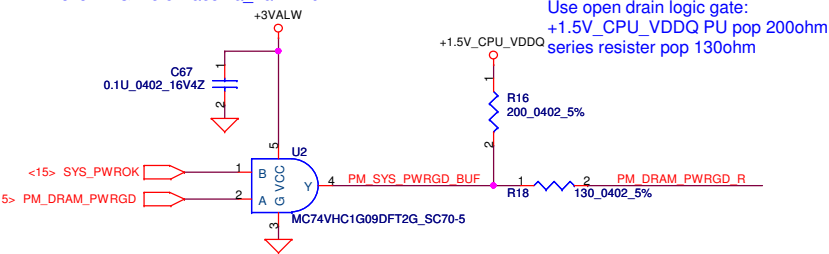
Follow DG 1.5 & Tacoma\_Fall2 1.0

Buffered reset to CPU



RESET#:都ok後請CPU做reset

Follow DG 1.5 & Tacoma\_Fall2 1.0



PROC\_SELECT#  
PH VCPLL and  
connect to PCH  
DF\_TVS

偵測CPU有無安裝  
XBOX 三紅功能

follow Checklist 1.5  
+1.05VS\_VTT

<18,35> H\_PECI  
H\_PECI  
<35> H\_PROCHOT#  
H\_PROCHOT#

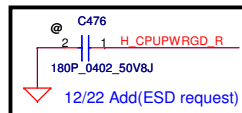
<18> H\_THERMTRIP#

<15> H\_PM\_SYNC

UNCOREPWROK:非CORE外的電OK  
SM\_DRAMPWROK:DRAM power ok

BUF\_CPU\_RST#

0.1\_10  
C105  
180P\_0402\_50V8J



12/22 Add(ESD request)

UCPU1B

PROC\_SELECT#

PROC\_DETECT#

CATERR#

PECI

PROCHOT#

THERMTRIP#

PM\_SYNC

UNCOREPWROK

SM\_DRAMPWROK

RESET#

IV-BRIDGE\_BGA1023

C867@

MISC

CLOCKS

DDR3

MISC

JTAG & BPM

FWR MANAGEMENT

+1.05VS\_VTT  
CLK\_CPU\_DPLL# R4 2 1K 0402 5%  
CLK\_CPU\_DPLL R5 2 1K 0402 5%  
Checklist1.5 P.67 Graphis Disable Guide  
eDP disable:  
DPLL\_REF\_SSCLK PD 1K\_5% to GND  
DPLL\_REF\_SSCLK# PU 1K\_5% to  
+1.05VS\_VTT

BCLK  
BCLK#  
DPLL\_REF\_CLK  
DPLL\_REF\_CLK#

SM\_RCOMP0,SM\_RCOMP1  
W=20mil L=500mil S=13mil

SM\_RCOMP2  
W=15mil  
L=500mil  
S=13mil

SM\_DRAMRST#  
SM\_DRAMRST# <6>

SM\_RCOMP0 R9 2 140 0402 1%  
SM\_RCOMP1 R10 2 25.5 0402 1%  
SM\_RCOMP2 R11 2 200 0402 1%

DDR3 Compensation Signals

PRDY#  
PREQ#

TCK  
TMS  
TRST#

TDI  
TDO

DBR#  
XDP\_DBRESET# <15>

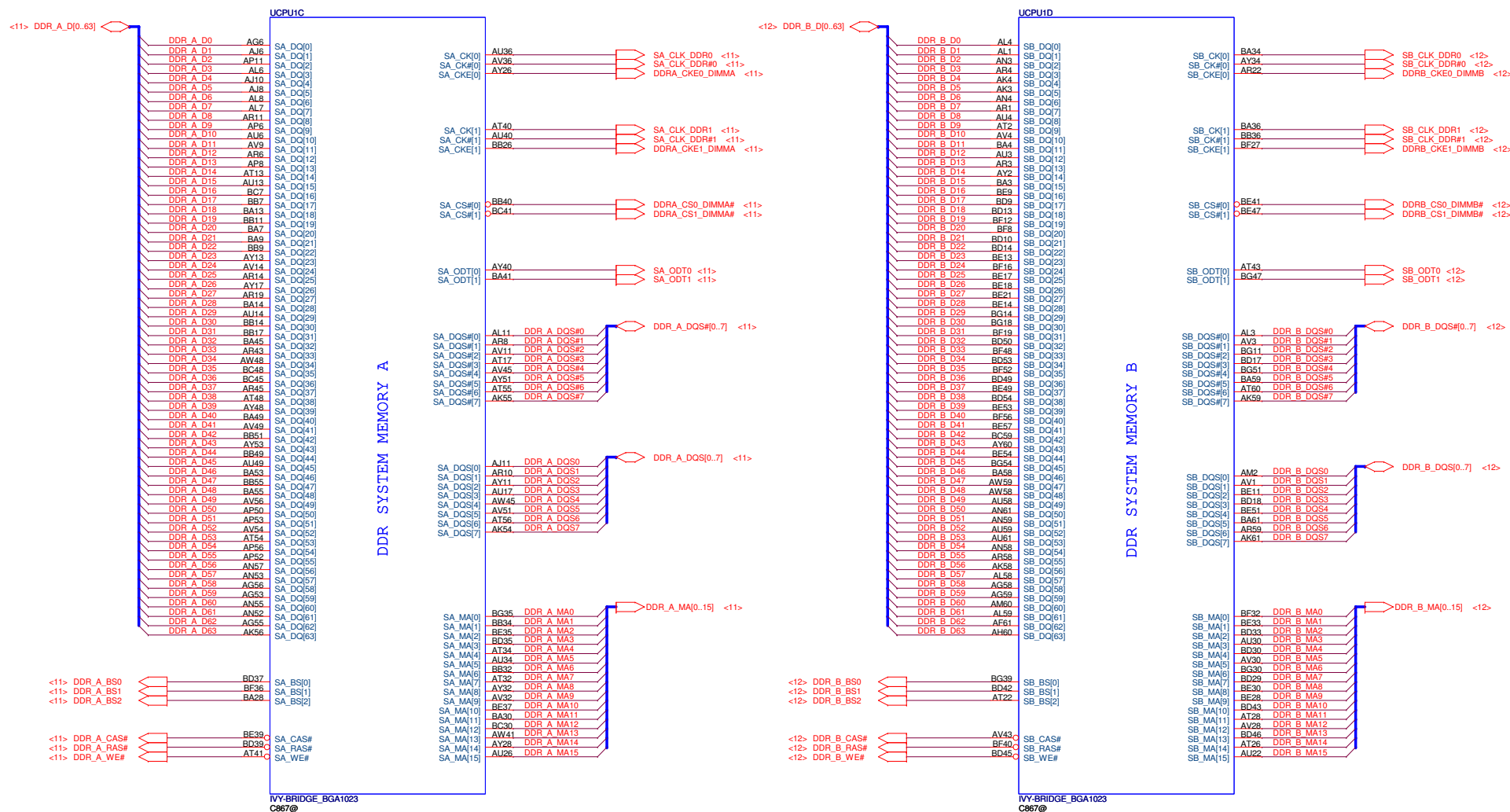
BPM#0  
BPM#1  
BPM#2  
BPM#3  
BPM#4  
BPM#5  
BPM#6  
BPM#7

G58  
E55  
E59  
G55  
G59  
H60  
J59  
J61

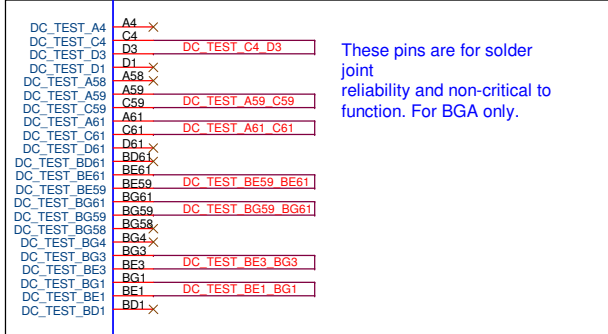
XDP\_DBRESET# R17 2 1K 0402 5%  
Tacoma\_Fall2 1.0 PU 1K +3VS  
Check list 1.5 PU 1K +3VS  
Debug port DG1.1-1.3 50~5K  
ohm

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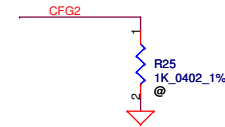


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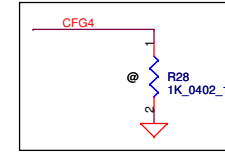


These pins are for solder joint reliability and non-critical to function. For BGA only.

## CFG Straps for Processor

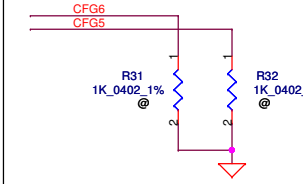


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition ★ 0: Lane Reversed

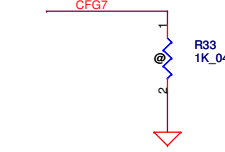


UMA,Optimus eDP啟動  
DISO eDP關閉

eDP enable	
CFG4	★ 1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) 1x16 PCI Express ★ 10: 2x8 PCI Express 01: Reserved 00: 1x8,2x4 PCI Express

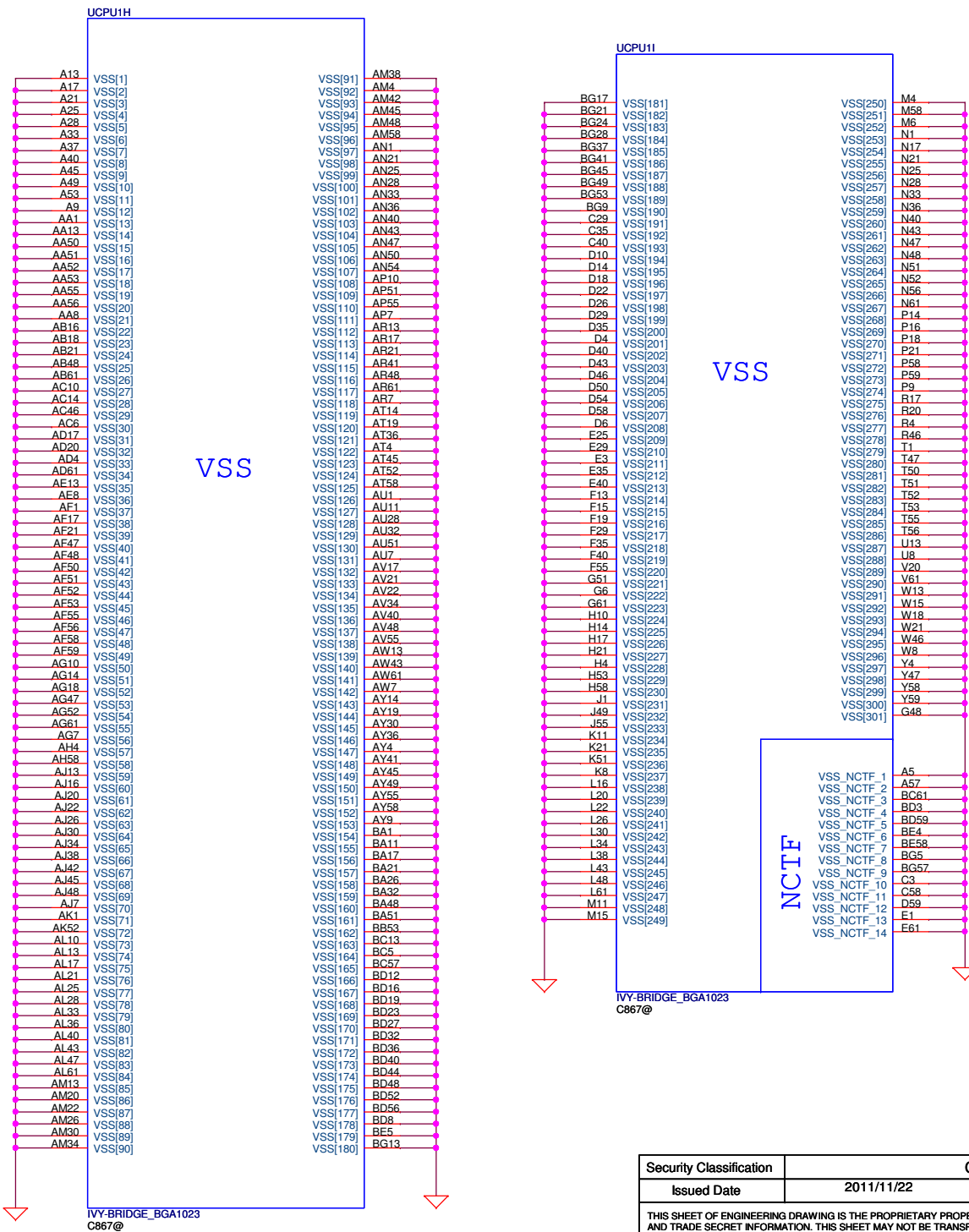


PEG DEFER TRAINING	
CFG7	Tacoma_Fall2 1.0 P.12 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



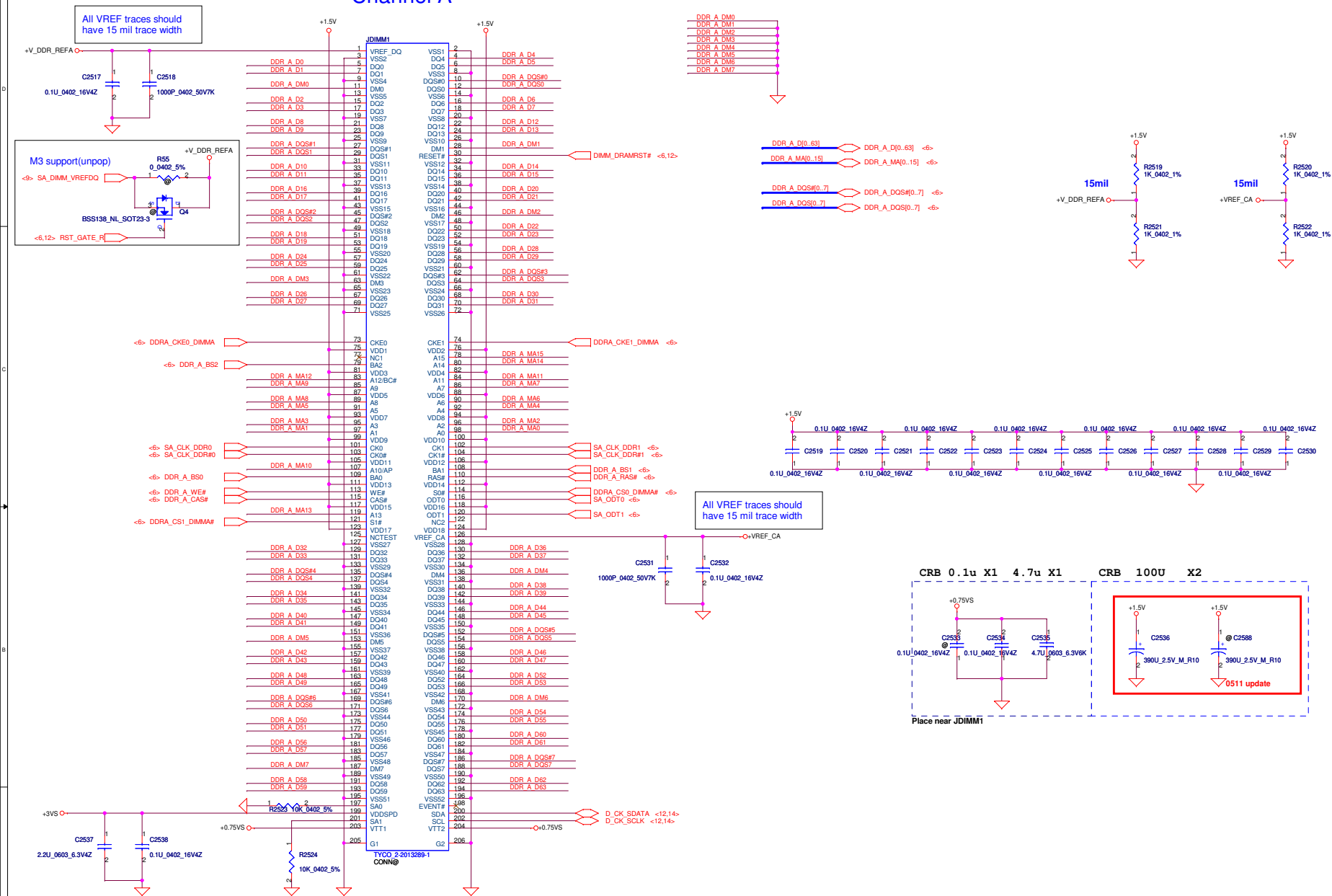






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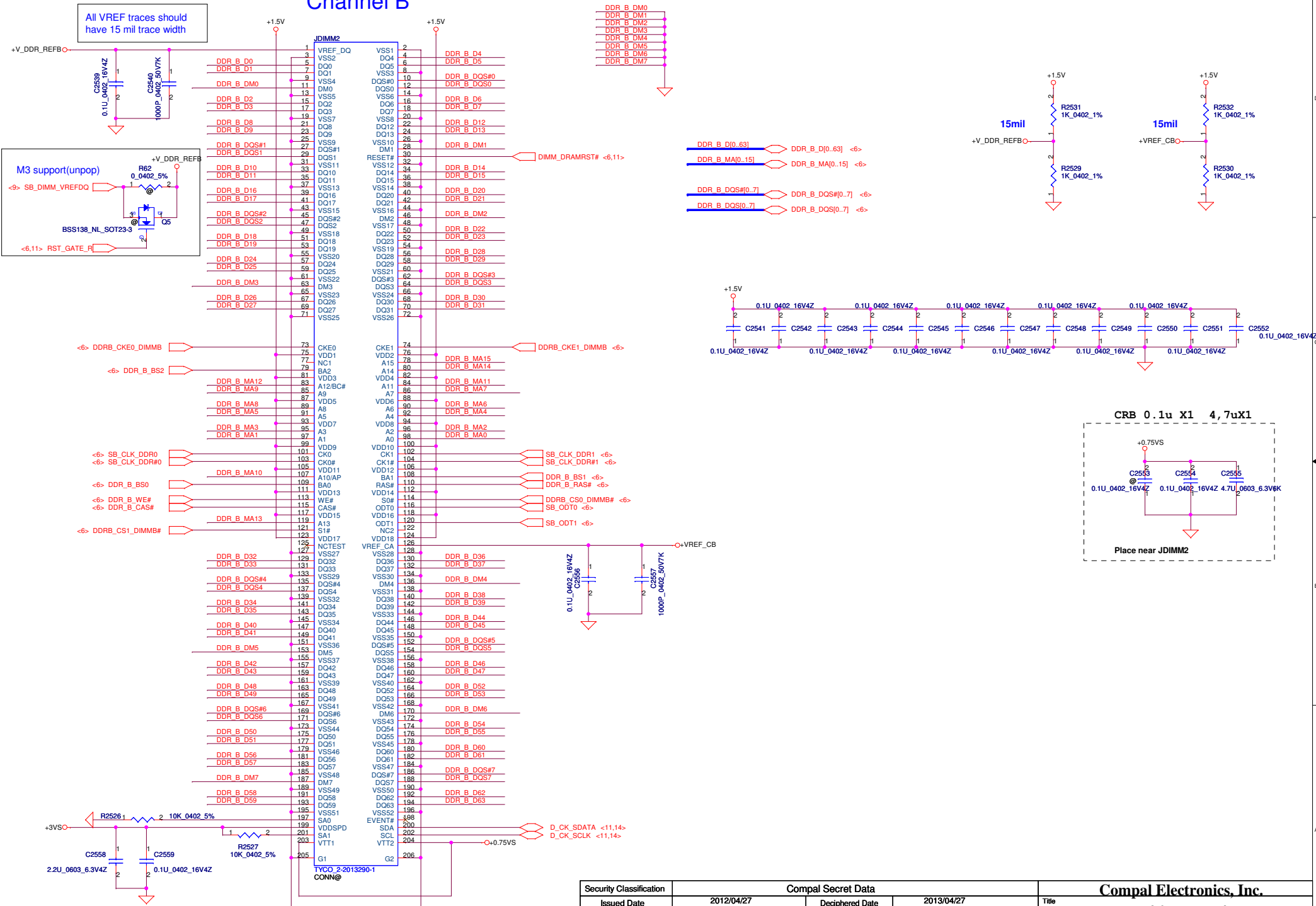
## Channel A



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						DDR3 SODIMM-I Socket					
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# Channel B



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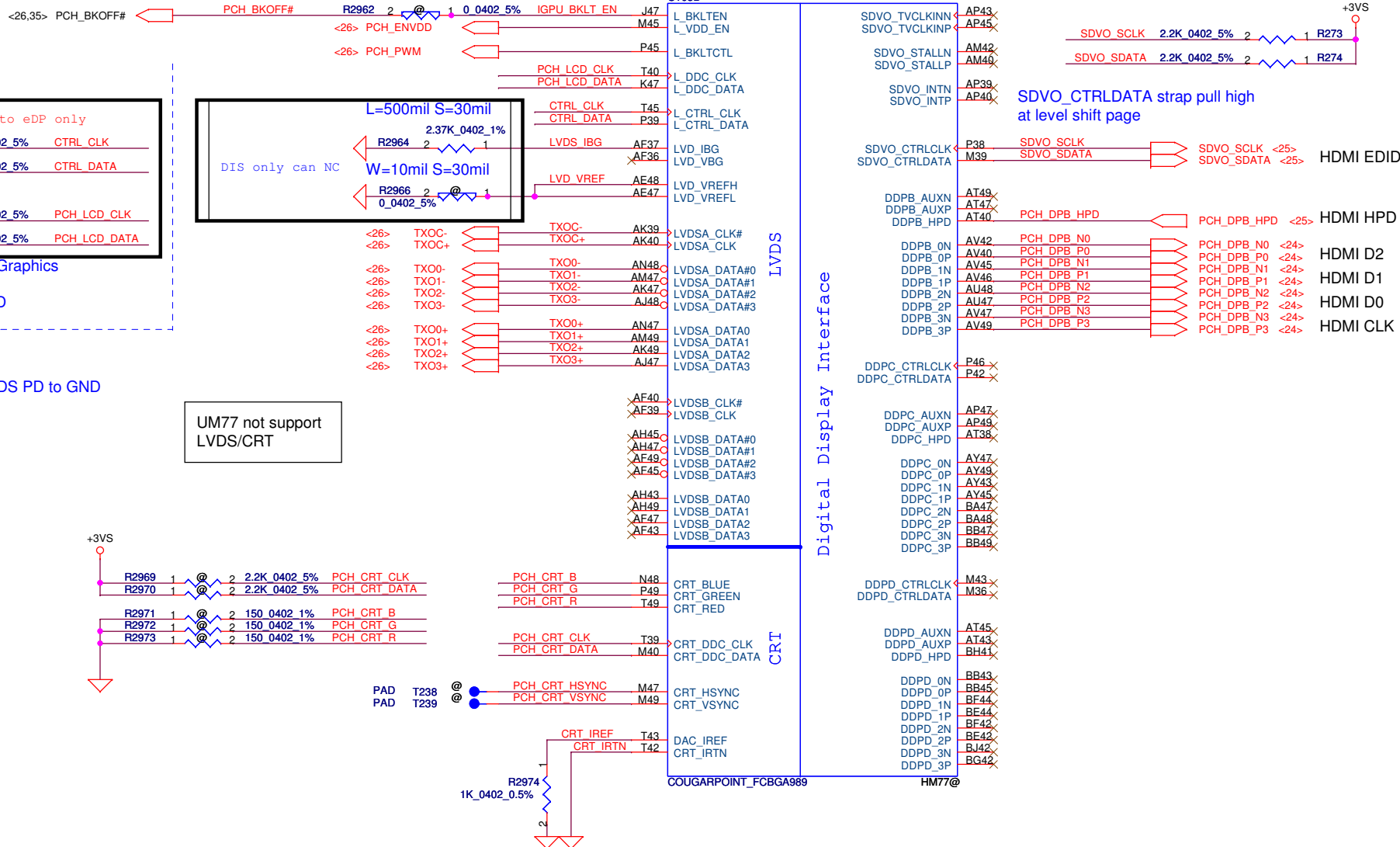








# UMA Panel Backlight ON/OFF



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										PCH (4/9) LVDS,CRT,DP,HDMI	
										Size	Document Number
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HDA\_SYNC PH(PLL =+1.5VS)

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up  
\* On-Die PLL voltage regulator enable  
L On-Die PLL Voltage Regulator disable

+VCCSUS3\_3

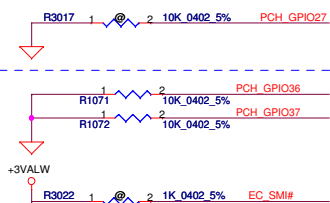


Fan Tachometer Inputs  
TACH1~7 only on  
server  
can insted to GPIO

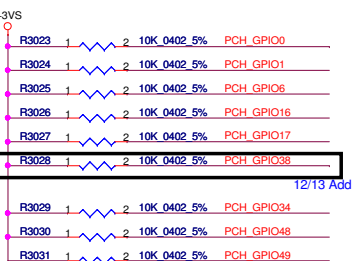
No use PU 10K +3VS	PCH_GPIO0	T7
No use PU 10K +3VS	PCH_GPIO1	A42
No use PU 10K +3VS	PCH_GPIO6	H36
No use PU 10K +3VS	<35> EC_SCI#	E38
No use PU 10K +3VALW	<35> EC_SMI#	C10
No use PU +3VALW	PCH_GPIO12	C4
No use PU +3VALW	PCH_GPIO15	G2
No use PU +3VS	PCH_GPIO16	U2
No use PU +3VS	PCH_GPIO17	D40
No use PU 10K +3VS	PCH_GPIO22	T5
No use PU +3VALW	PCH_GPIO24	E8
No use PU 10K +3VALW	PCH_GPIO27	E16
No use PU 10K +3VS	PCH_GPIO28	P8
No use can NC	PAD T225@	K1
Can't PU	PCH_GPIO34	K4
Can't PU	PCH_GPIO35	K4
No use PU 10K +3VS	PCH_GPIO36	V8
No use PU 10K +3VS	PCH_GPIO37	M5
No use PU 10K +3VS	PCH_GPIO38	N2
No use PU 10K +3VS	PCH_GPIO39	M3
No use PU 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PU 10K +3VS	PCH_GPIO49	V3
No use PU +3VALW	PCH_GPIO57	D6

Deep S4,S5 wake event signal  
RTC alarm,Power  
BTN,GPIO27

PCH\_GPIO27 (Have internal Pull-High)  
Deep S4,S5 wake event signal



SATA2GP/GPIO36 &  
SATA3GP/GPIO37  
Sampled at Rising edge of  
PWROK.  
Weak internal pull-down.  
(weak internal pull-down is disabled  
after PLTRST# de-asserts)  
NOTE: This signal should NOT be  
pulled high when strap is sampled



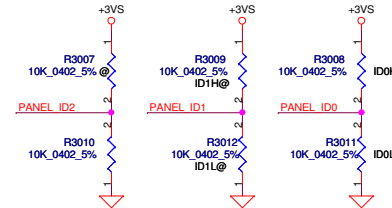
+VCCSUS3\_3



GPIO24 Unmultiplexed  
NOTE: GPIO24 configuration  
register bits are not cleared by  
CF9h reset event.  
CRB1.0 PU 10K to +3VALW

GPIO36/GPIO37 is Strap functionality  
that requires internal pull down to be sampled at rising PWROK.  
When uses as SATA2GP/SATA3GP for mechanical presence detect  
-use a external pull up 150K-200K ohm to Vcc3\_3  
When used as GP input  
-ensure GPI is not driven high during strap sampling window  
When Unused as GPIO or SATA\*GP  
-use 8.2K-10K pull-down  
check list page 47

PANEL ID

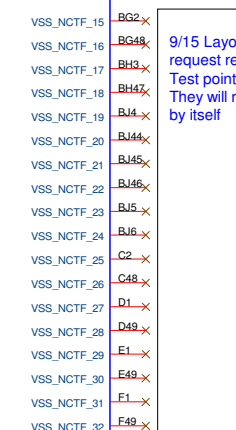
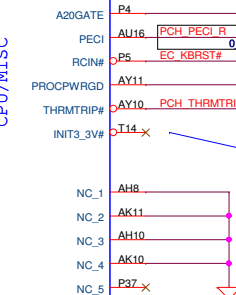
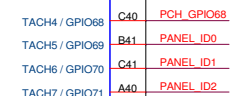


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0	0	0	CMI M185BGE-L22
0	0	1	AUO M185XTN01.2
0	1	0	LGD LM185WH2-TLK1
0	1	1	

GPIO

CPU/MISC

NCTF

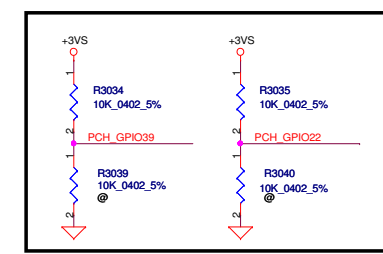
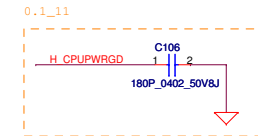


COUGARPOINT\_FCBGA969  
HM77@

PECI CPU-EC  
CTRL+ALT+DEL  
non CPU power ok  
130c shut down

INIT3\_3V  
This signal has weak internal  
PU, can't pull low,leave NC  
TS\_VSS1~4  
PD to GND

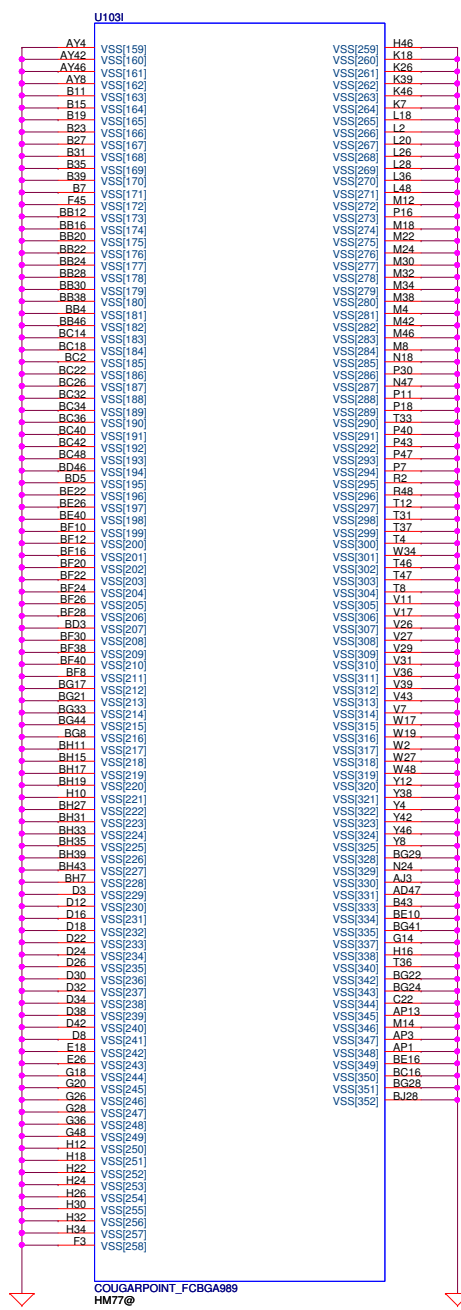
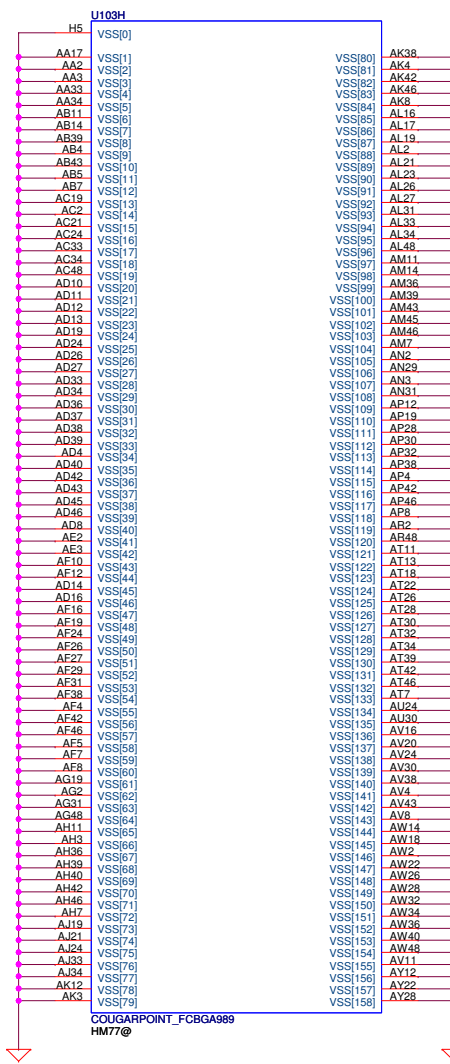
9/15 Layout  
request remove  
Test point  
They will route  
by itself



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				PCH (9/9) VSS	
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		Custom	VBA20 LA-9303P M/B	0.2	
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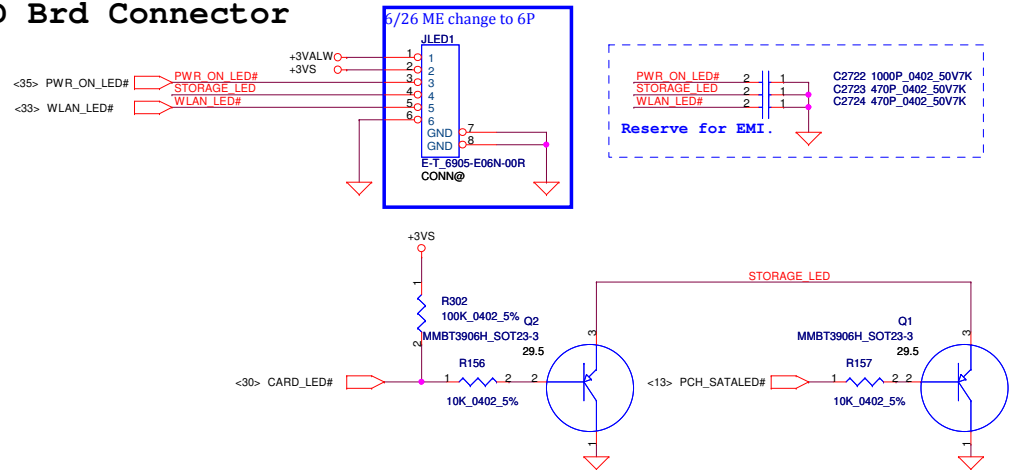
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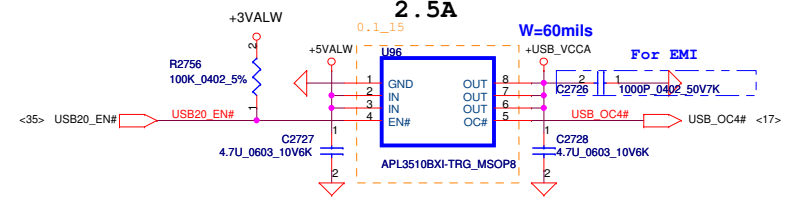
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LED Brd Connector

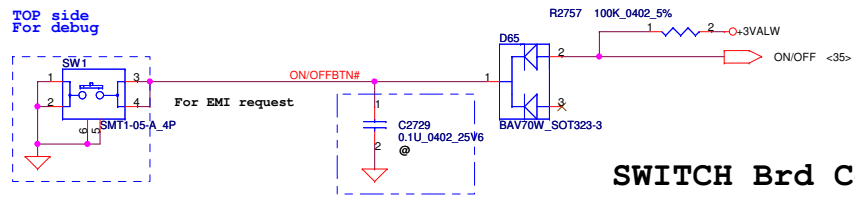


USB2.0 Power

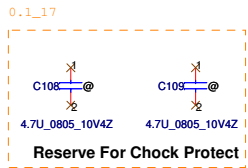
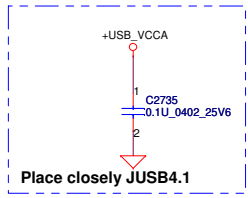
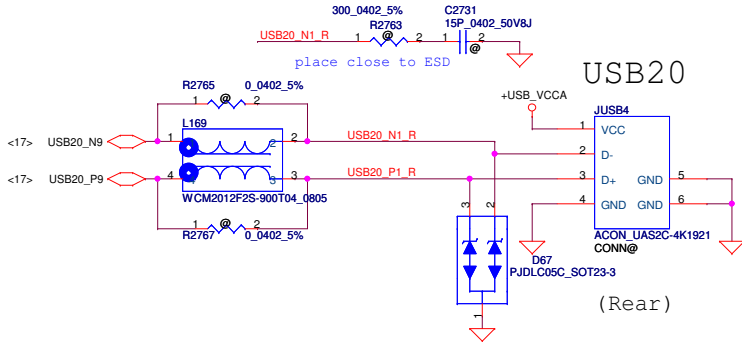
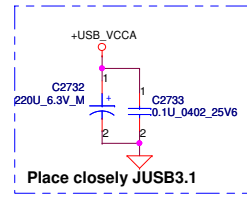
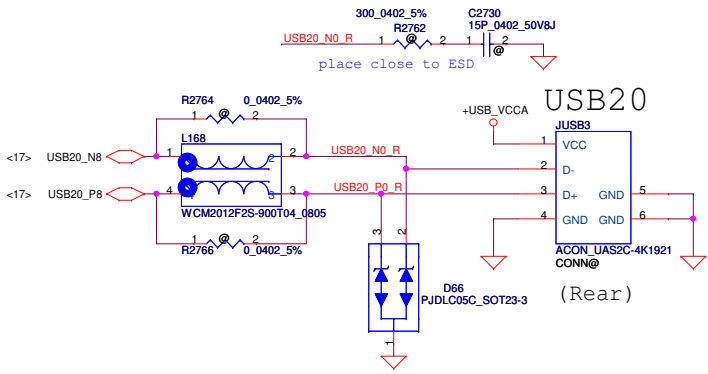
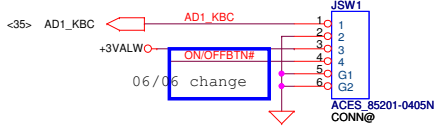
2.5A



SWITCH Brd Connector



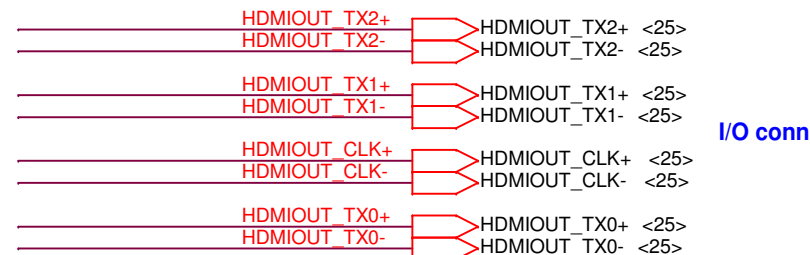
PU 4.7K on EC side



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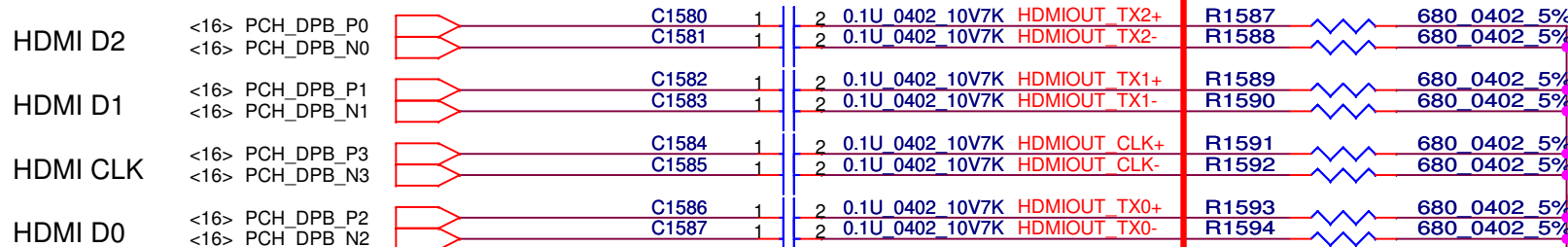
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# HDMI-OUT Level Shift

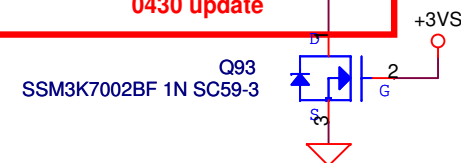


INTEL use 680 Ohm for terminationn

PCH



C & R close to J101 as short as possible



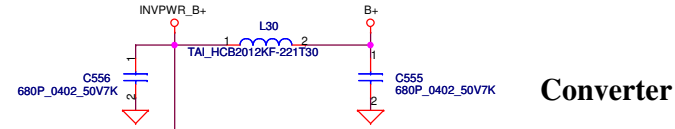
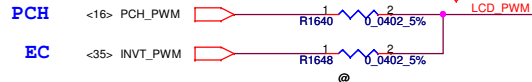




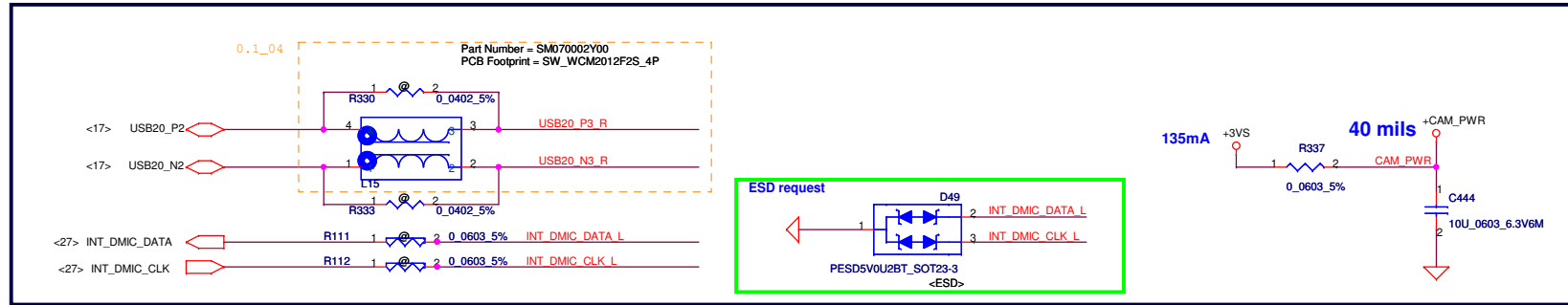
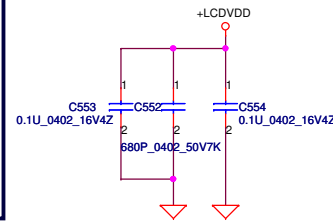
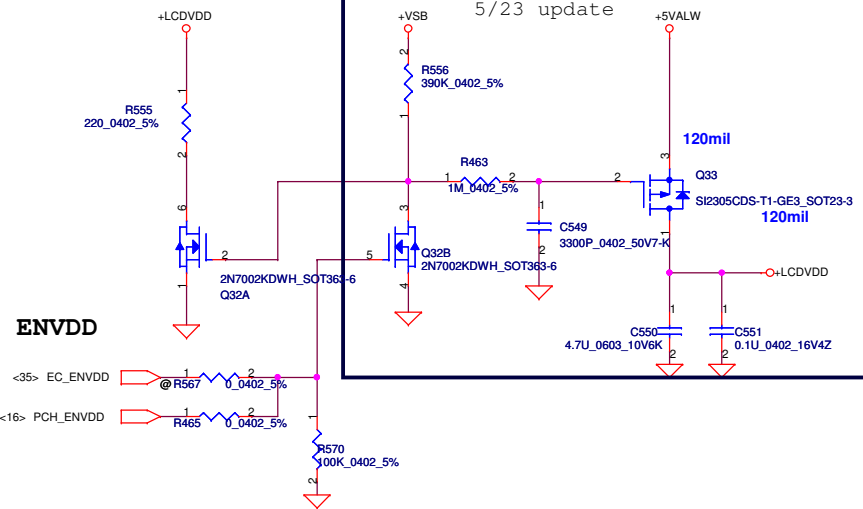
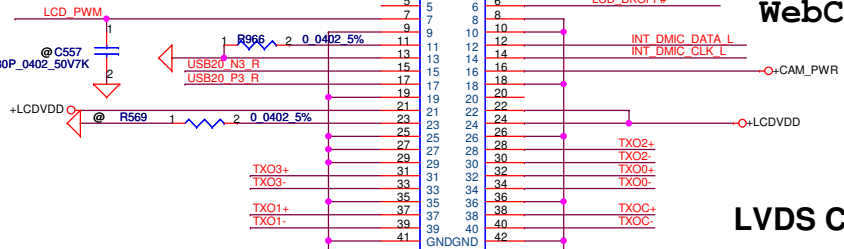
## BKOFF#



## PWM

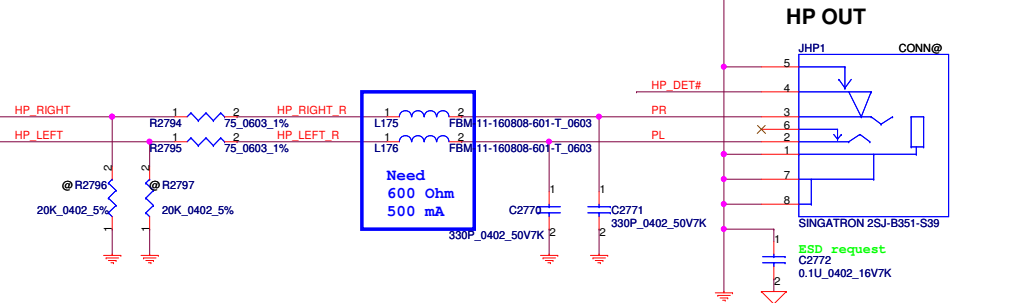
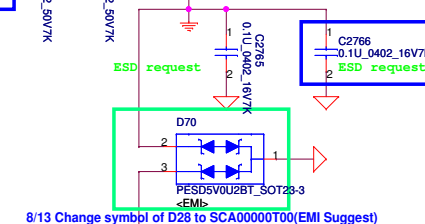
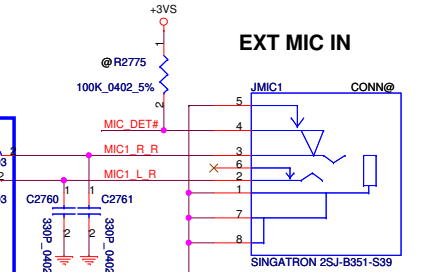
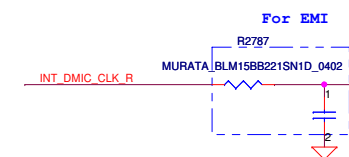
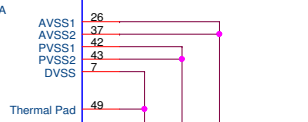
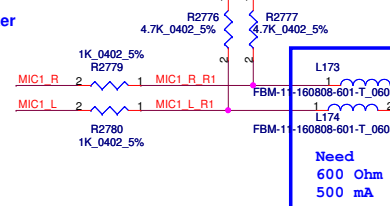
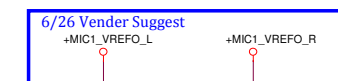
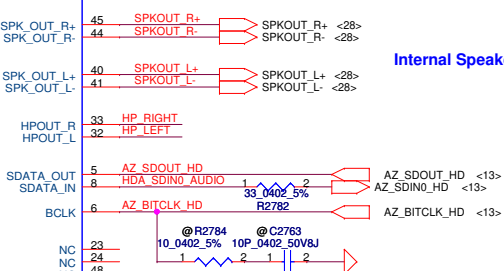
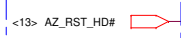
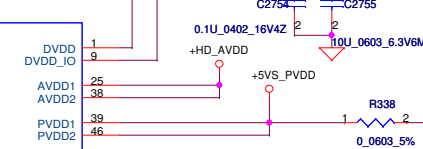
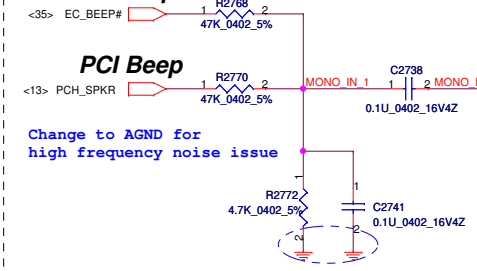
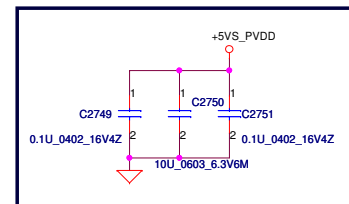
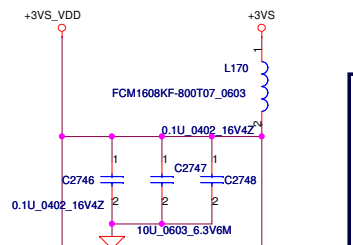
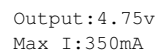


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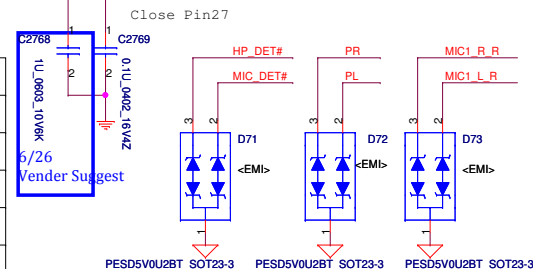


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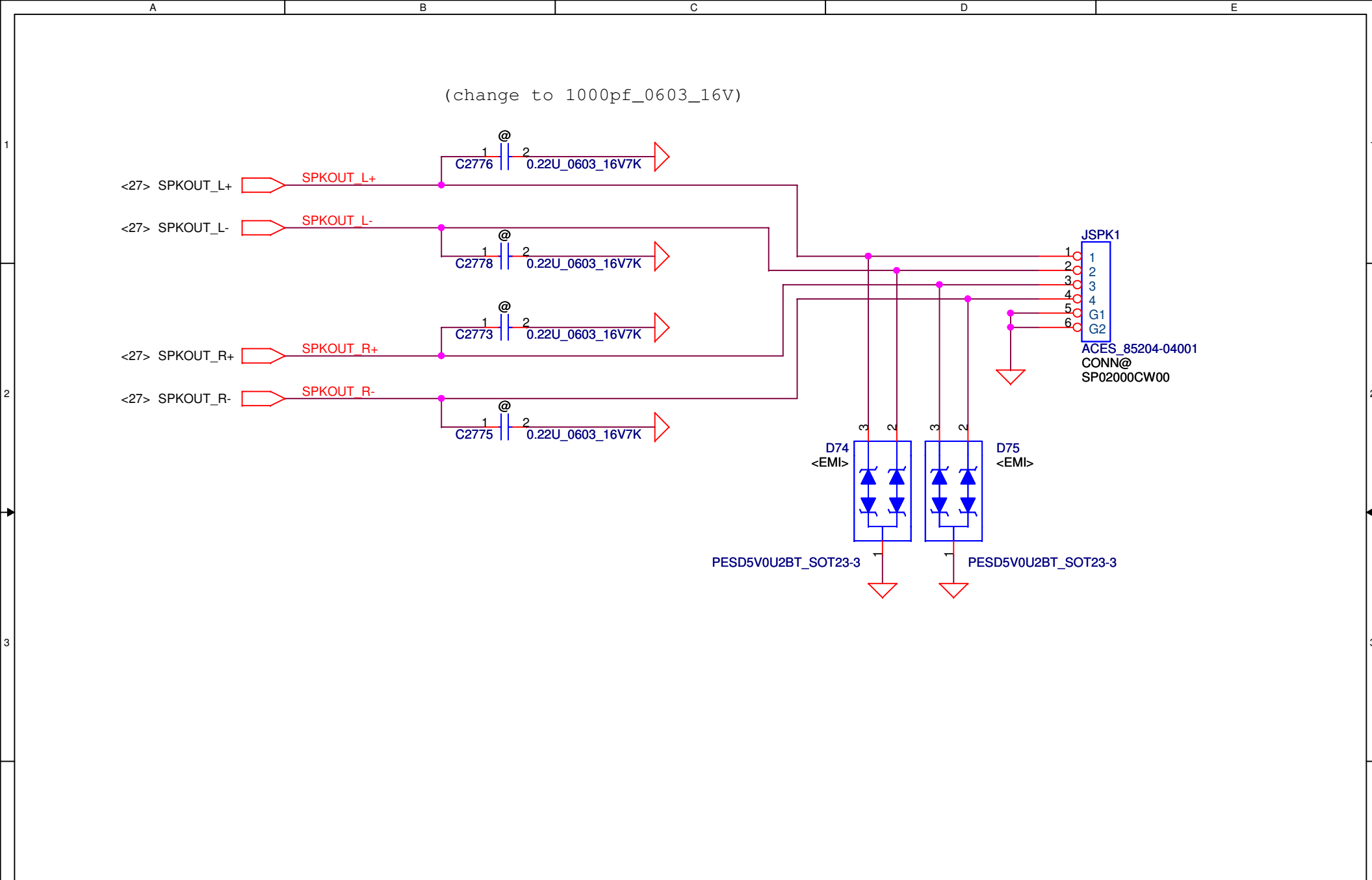


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	HP-OUT (PIN 32,33)
	20K	MIC1 (PIN 21, 22)
	10K	LINE1 (PIN 23, 24)
	5.1K	LOUT1 (PIN 35,36)
SENSE B	39.2K	LINE2 (PIN 14, 15)
	20K	MIC2 (PIN 16, 17)
	5.1K	



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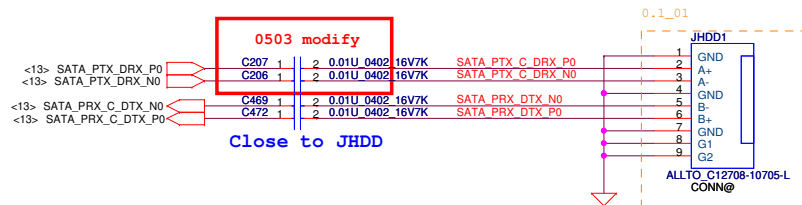
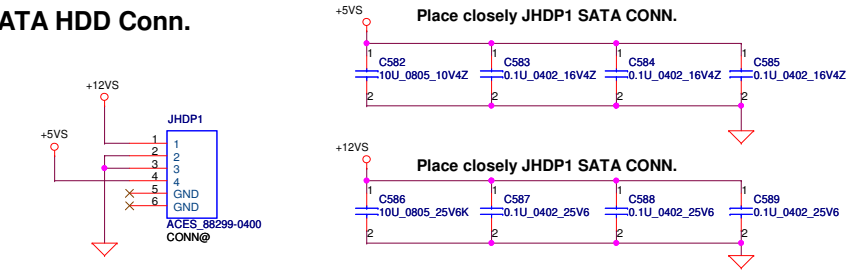
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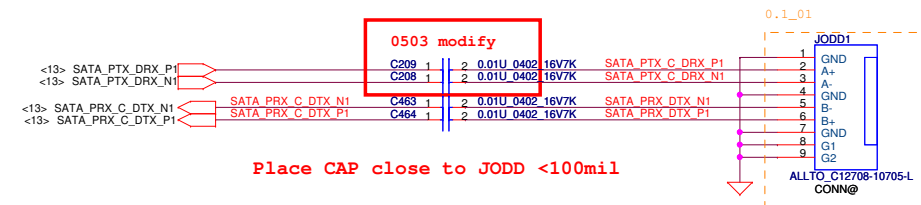
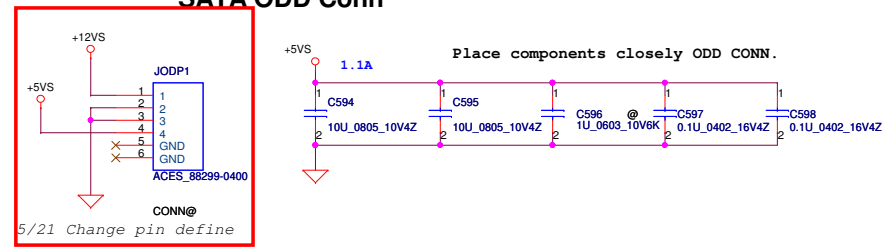
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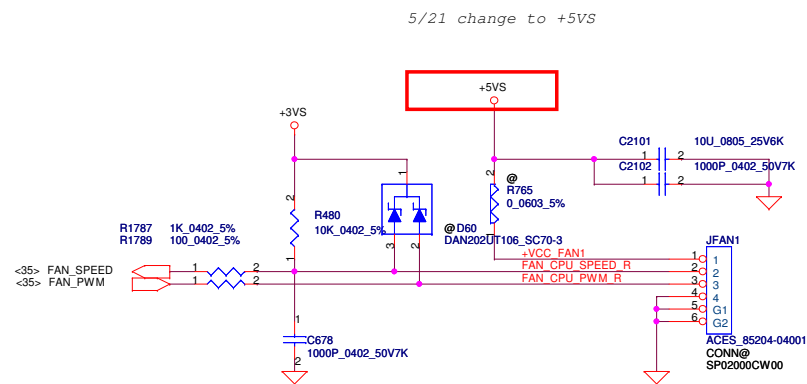
## SATA HDD Conn.



## SATA ODD Conn

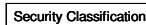
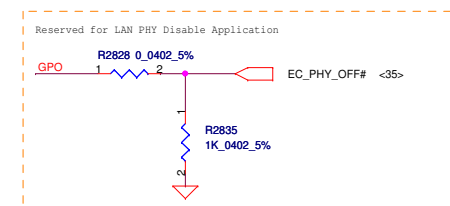


## FAN Control Circuit



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<b>LAN&amp;C</b>	
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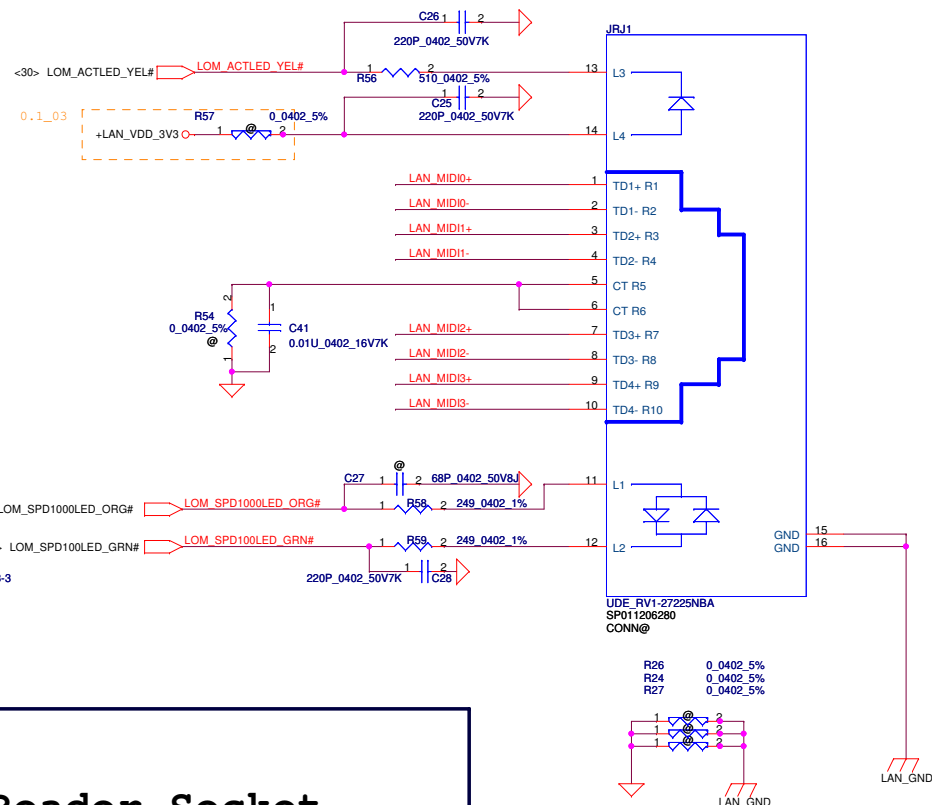
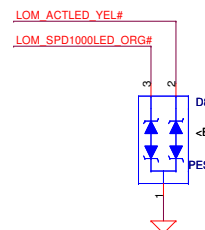
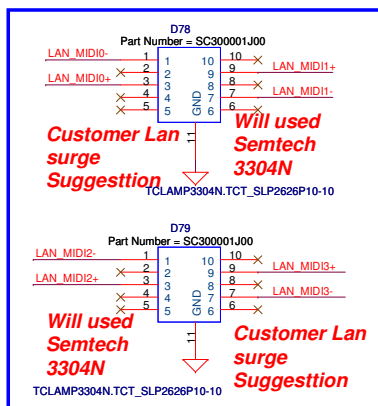
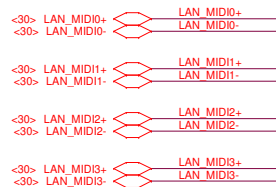
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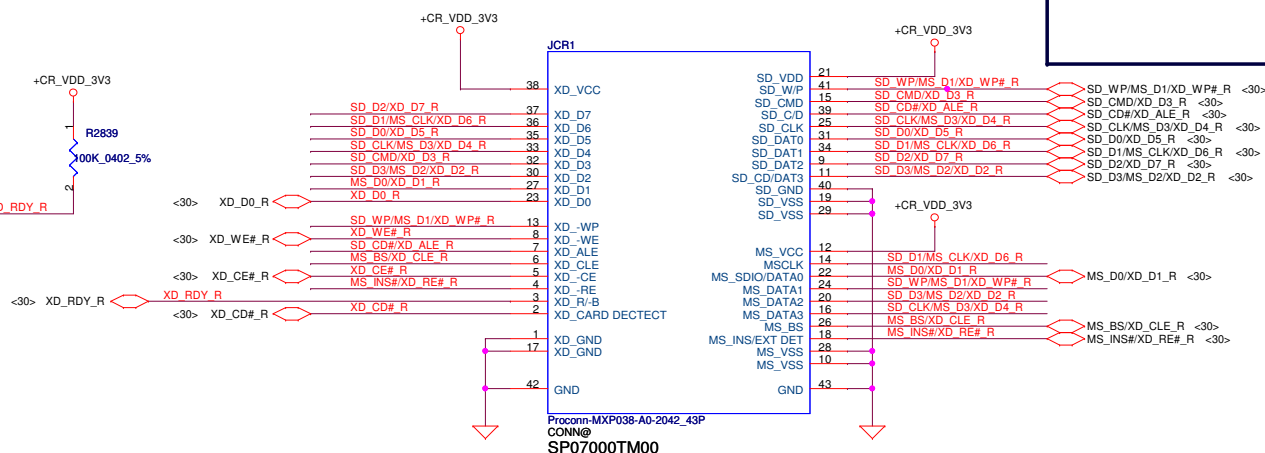
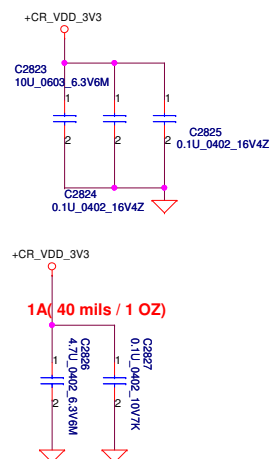
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## Combine Transformer to RJ45 (0626)



## Card Reader Socket



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Compal Electronics, Inc.

JMB385 Media Card Controller

Document Number

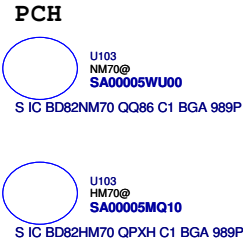
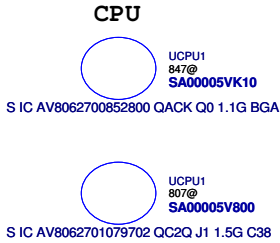
VBA20 LA-9303P M/B

Rev

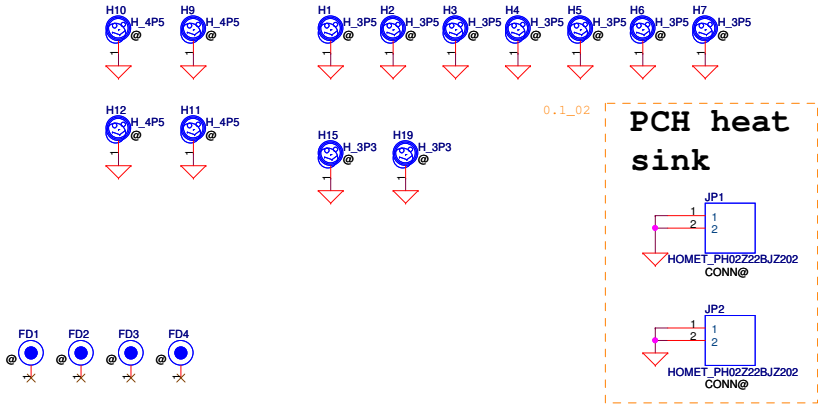
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ISPD



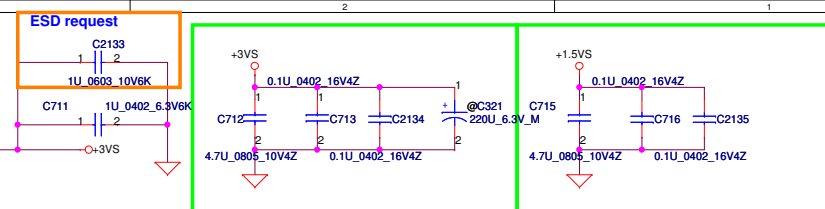
Screw Hole



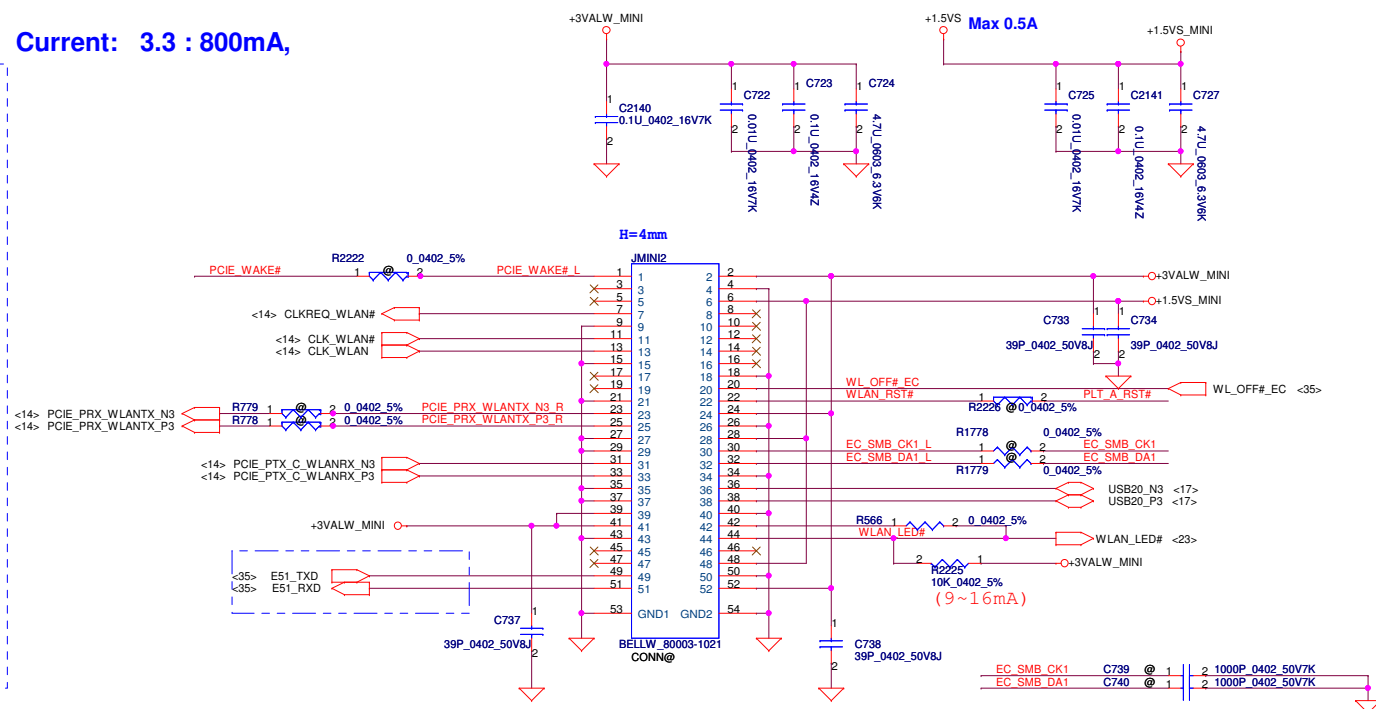
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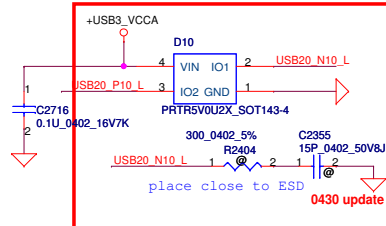
**Mini Card Slot 1---TV tuner Current: 3.3 : 2750mA, 1.5: 500mA**



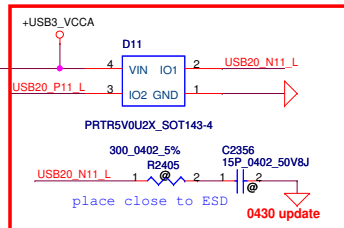
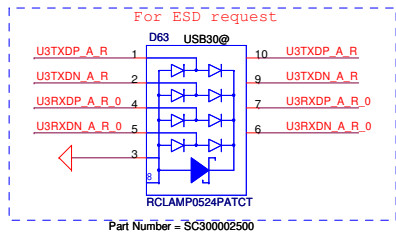
**Mini Card Slot 2--- WLAN Current: 3.3 : 800mA,**



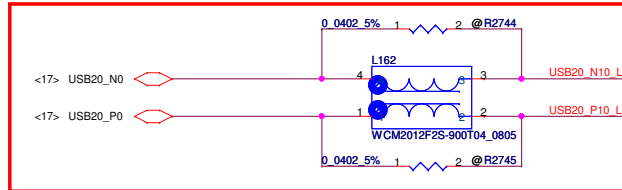
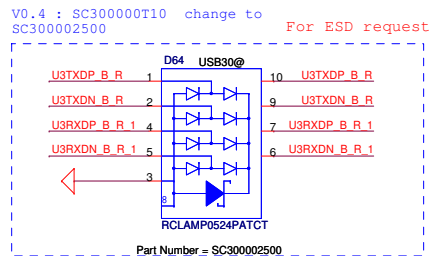
<http://sualaptop365.edu.vn>



V0.4 : SC300000T10 change to SC300002500



20101118 modify  
BOM USB30@->  
Normal (EMI part)

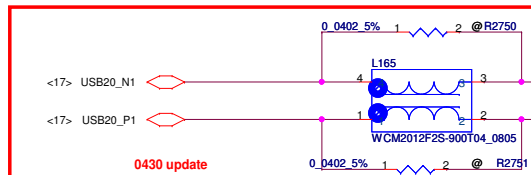
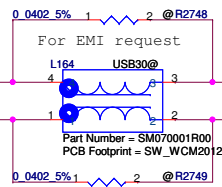
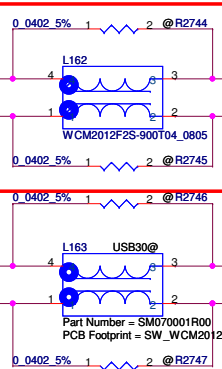


<17> PCH\_USB3\_RX1\_N

<17> PCH\_USB3\_RX1\_P

<17> PCH\_USB3\_TX1\_N

<17> PCH\_USB3\_TX1\_P

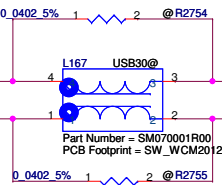
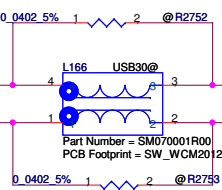


<17> PCH\_USB3\_RX2\_N

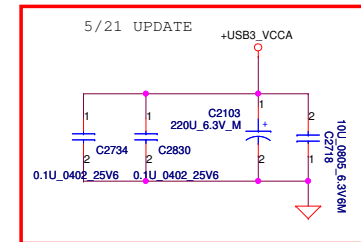
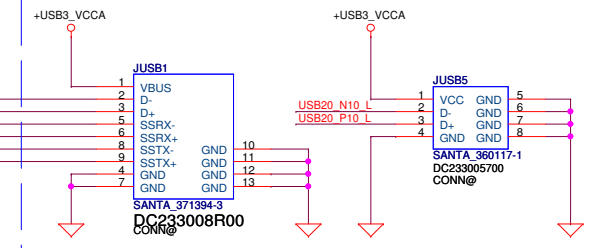
<17> PCH\_USB3\_RX2\_P

<17> PCH\_USB3\_TX2\_N

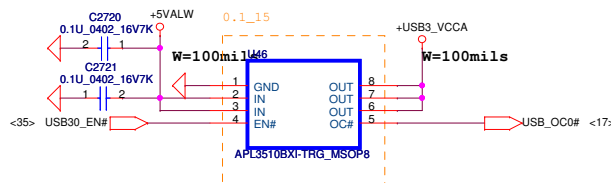
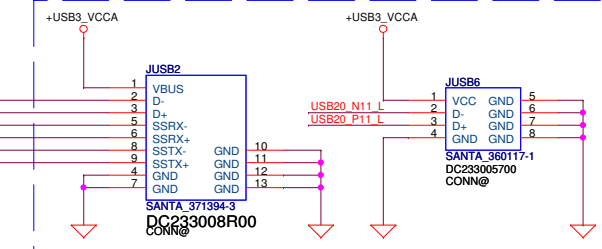
<17> PCH\_USB3\_TX2\_P



Co-Layout



Co-Layout

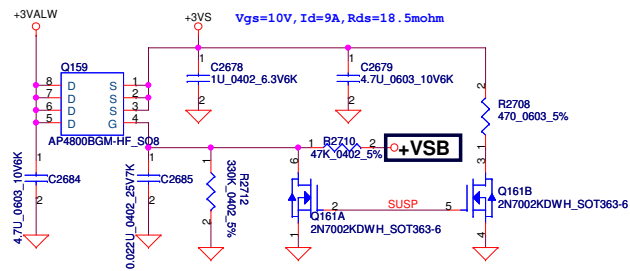


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Issued Date		Deciphered Date		Title	
				USB 3.0 CONN	
				Size	
				Document Number	
				VBA20 LA-9303P M/B	
				Rev	
				0.2	
				Date:	
				Sheet 34 of 49	

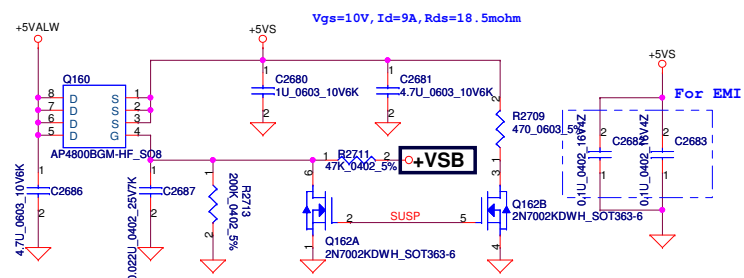
<http://sualaptop365.edu.vn>



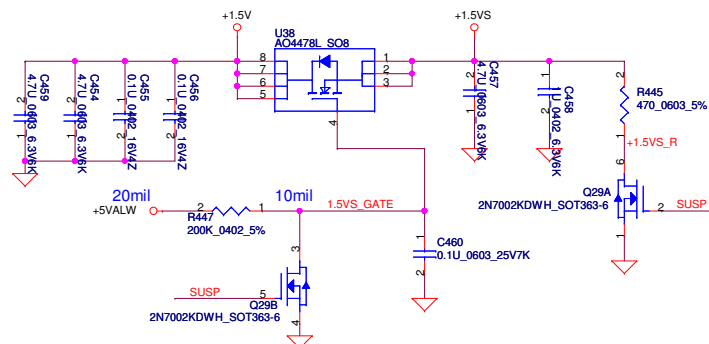
**+3VALW TO +3VS**



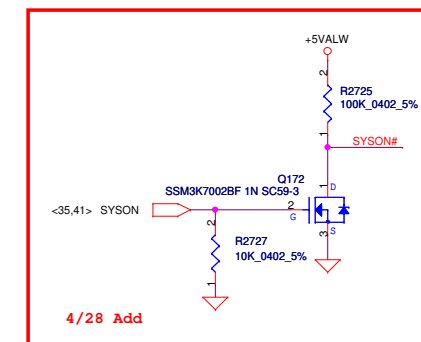
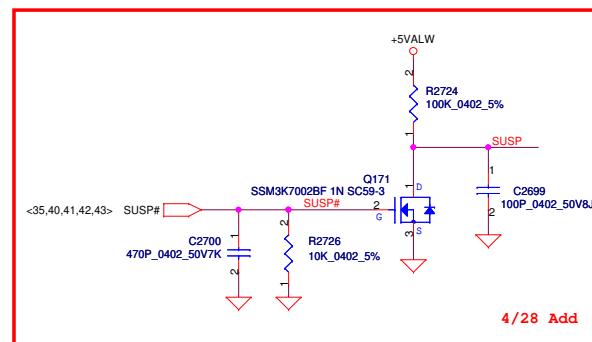
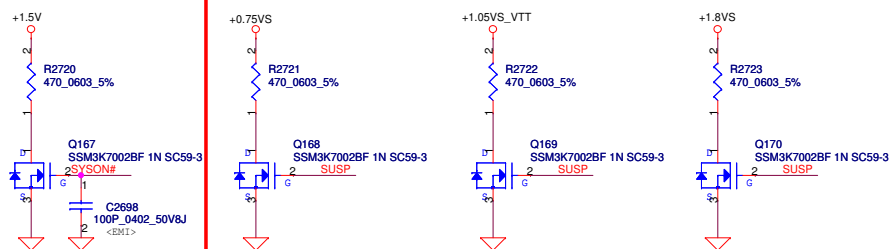
**+5VALW TO +5VS**



**+1.5V to +1.5VS**

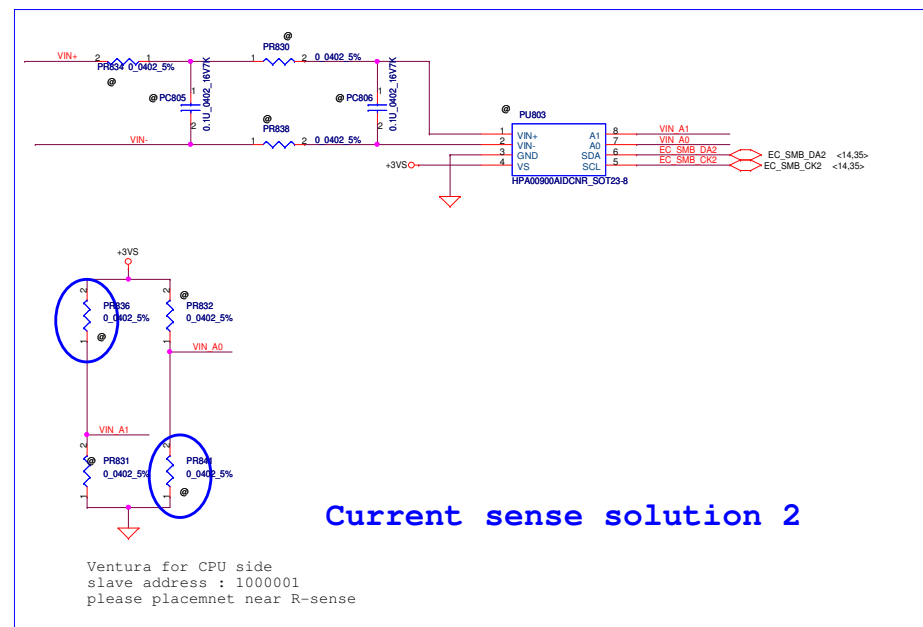
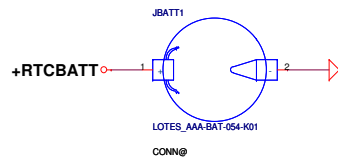


## Discharge circuit



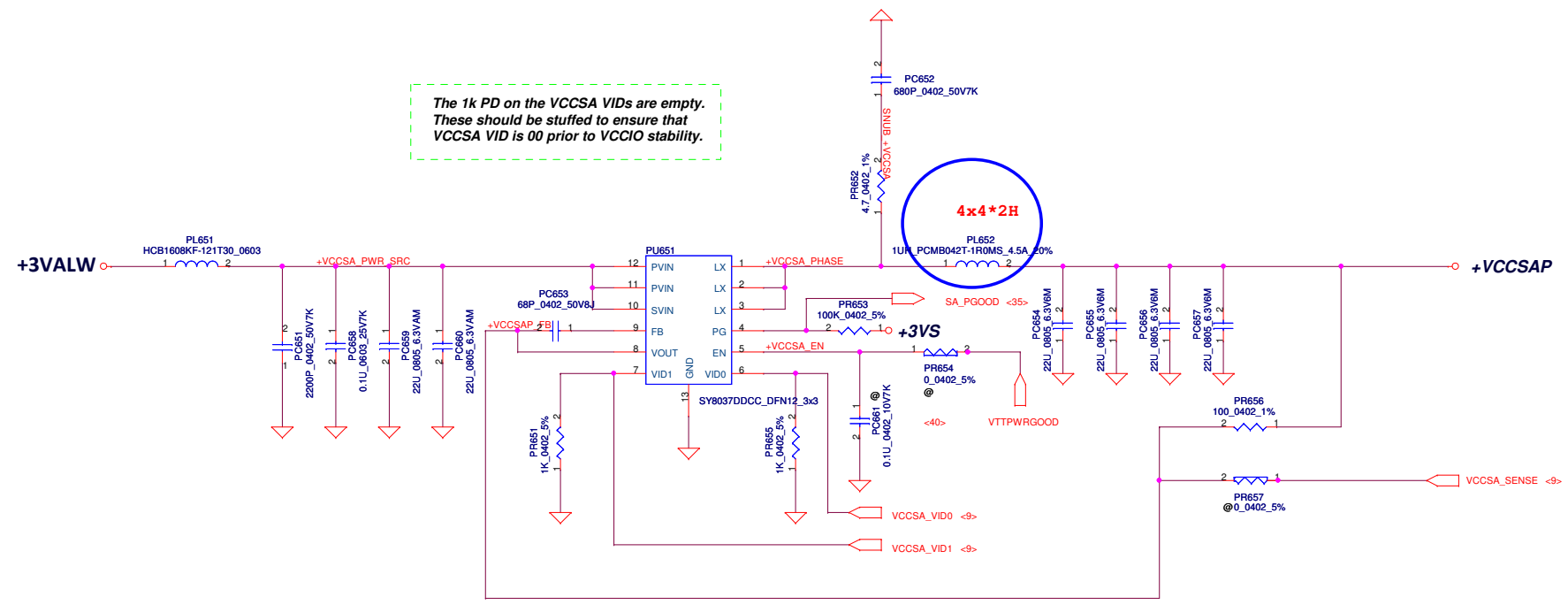
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>DC-DC INTERFACE/Discharge</b>	
Issued Date	2012/04/27	Deciphered Date	2013/04/27	Title	
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The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.



VID [0]	VID[1]	VCCSA Vout (ULV only)
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

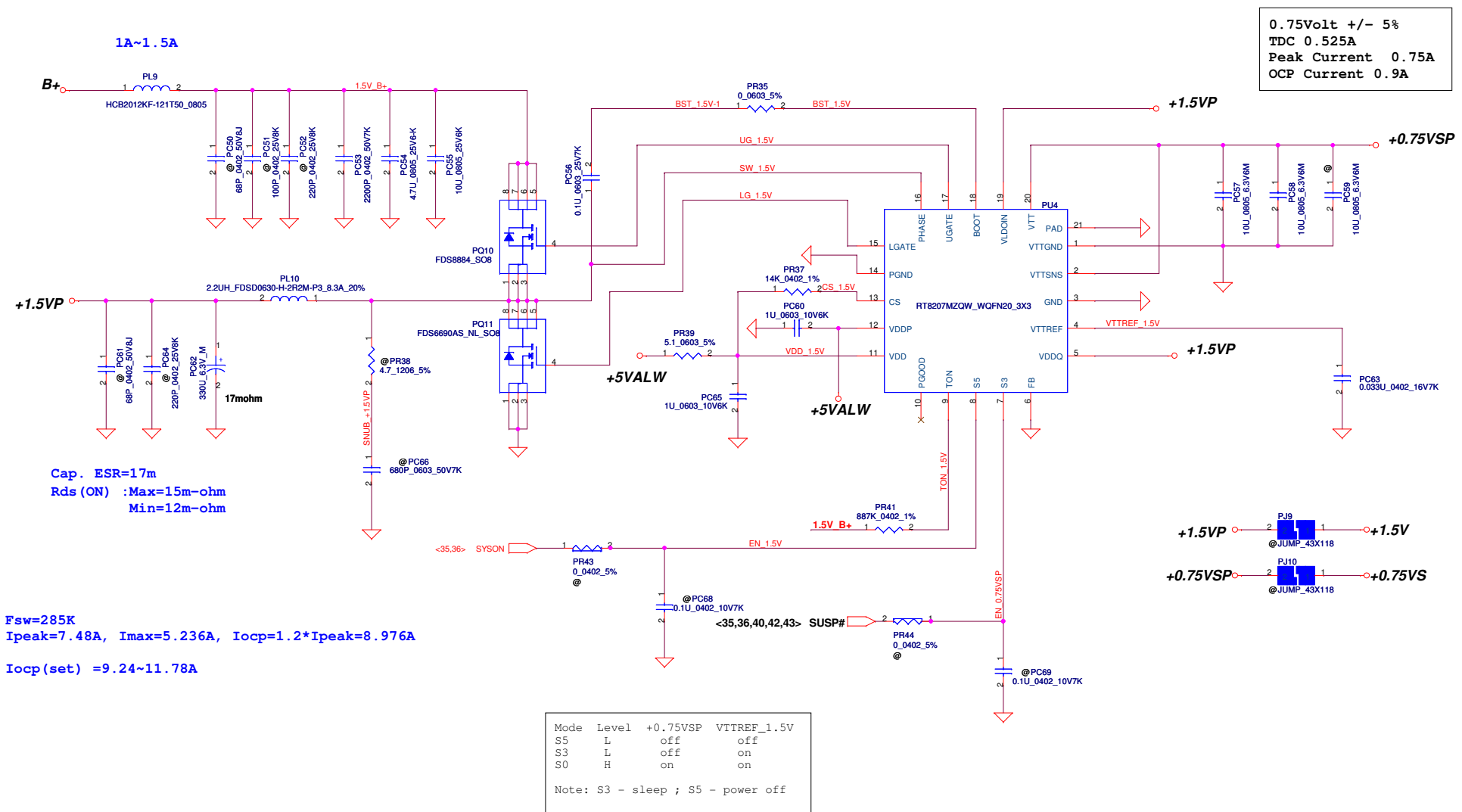
output voltage adjustable network

**+VCC\_SAP**  
**TDC 4.2A**  
**Peak Current 6A**  
**OCp current 7.2A**





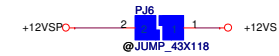
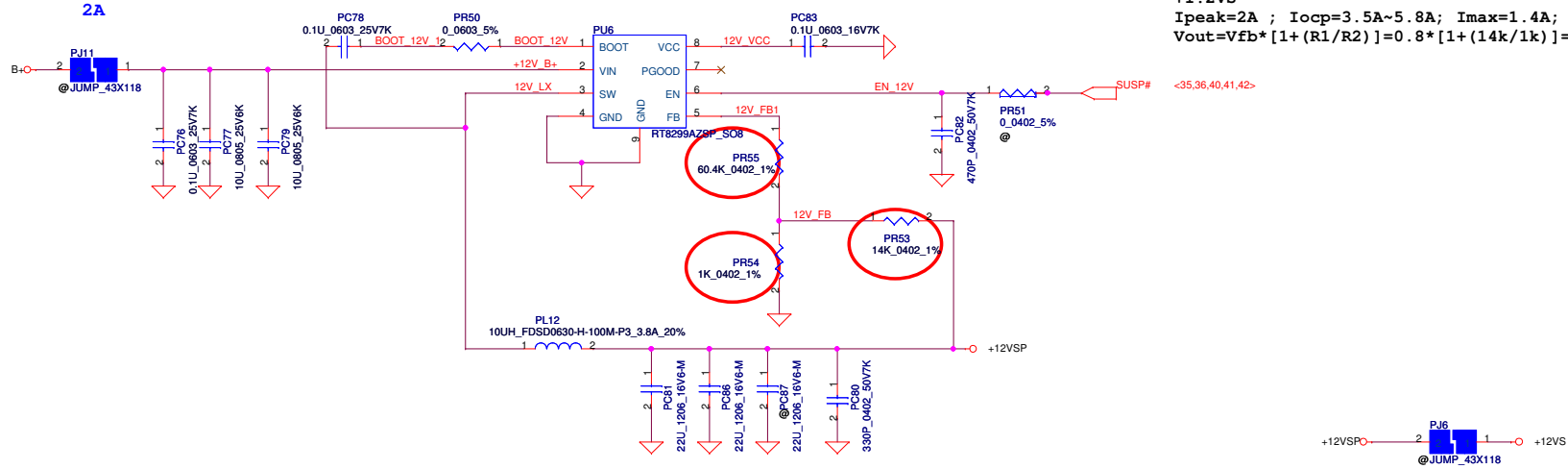


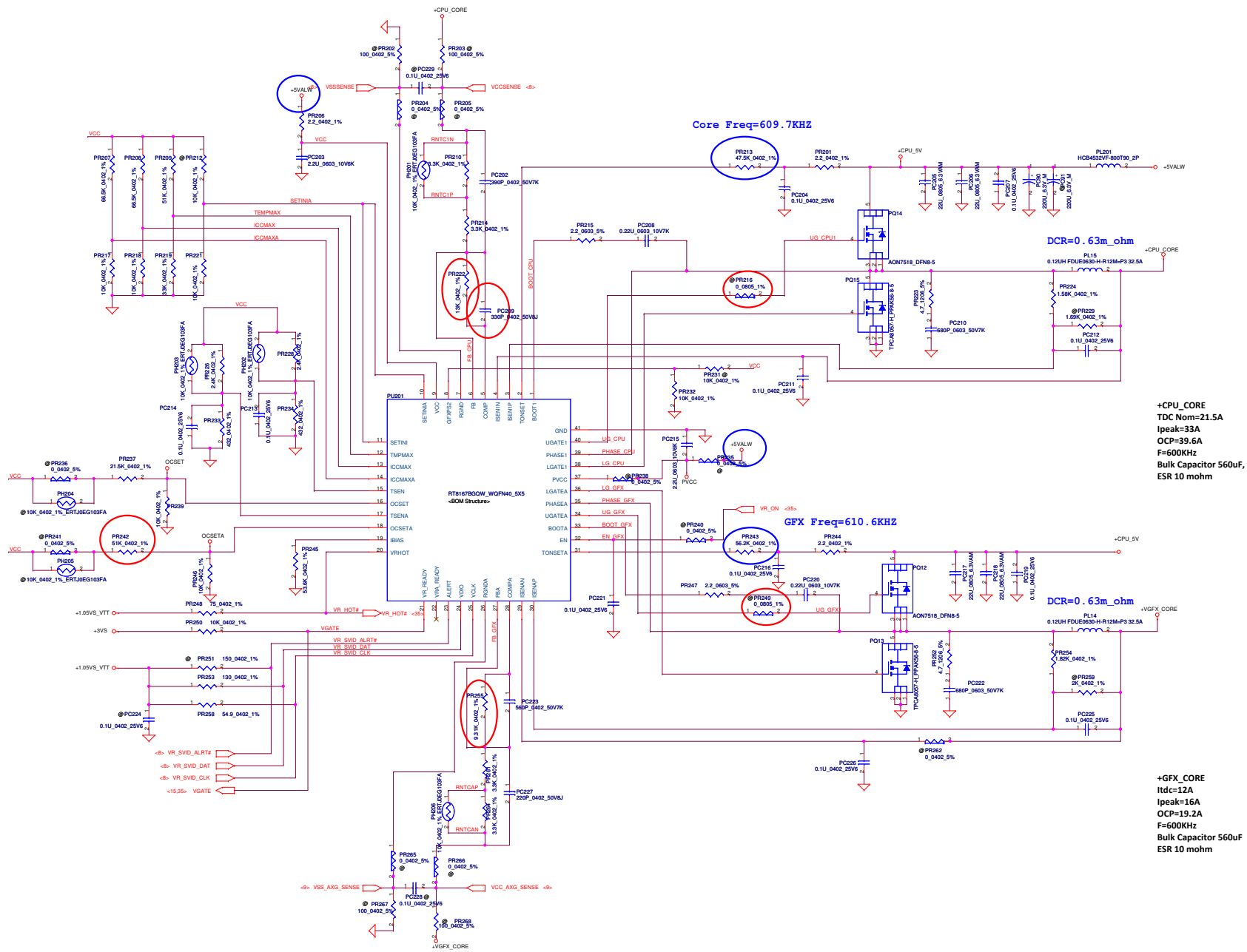




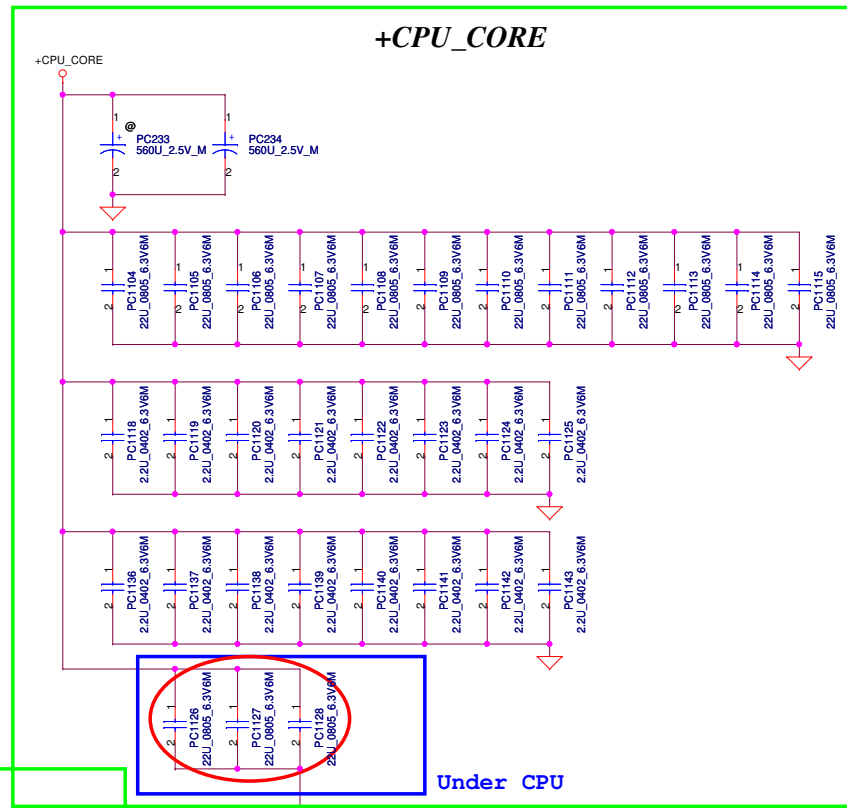
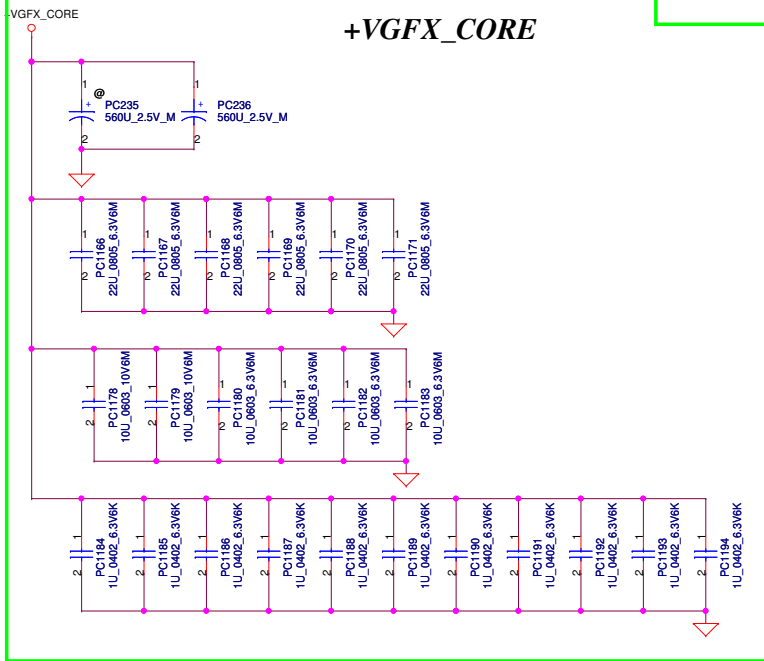
VFB=0.8V

+1.2VS  
 $I_{peak}=2A$  ;  $I_{ocp}=3.5A \sim 5.8A$ ;  $I_{max}=1.4A$ ;  $L=10\mu H$   
 $V_{out}=V_{fb} * [1 + (R1/R2)] = 0.8 * [1 + (14k/1k)] = 12V$





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				Date	Friday, August 10, 2012
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				Rev	0.1



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Size	Document Number	Rev			0.1
Date:	Friday, August 10, 2012	Sheet	45	of	48

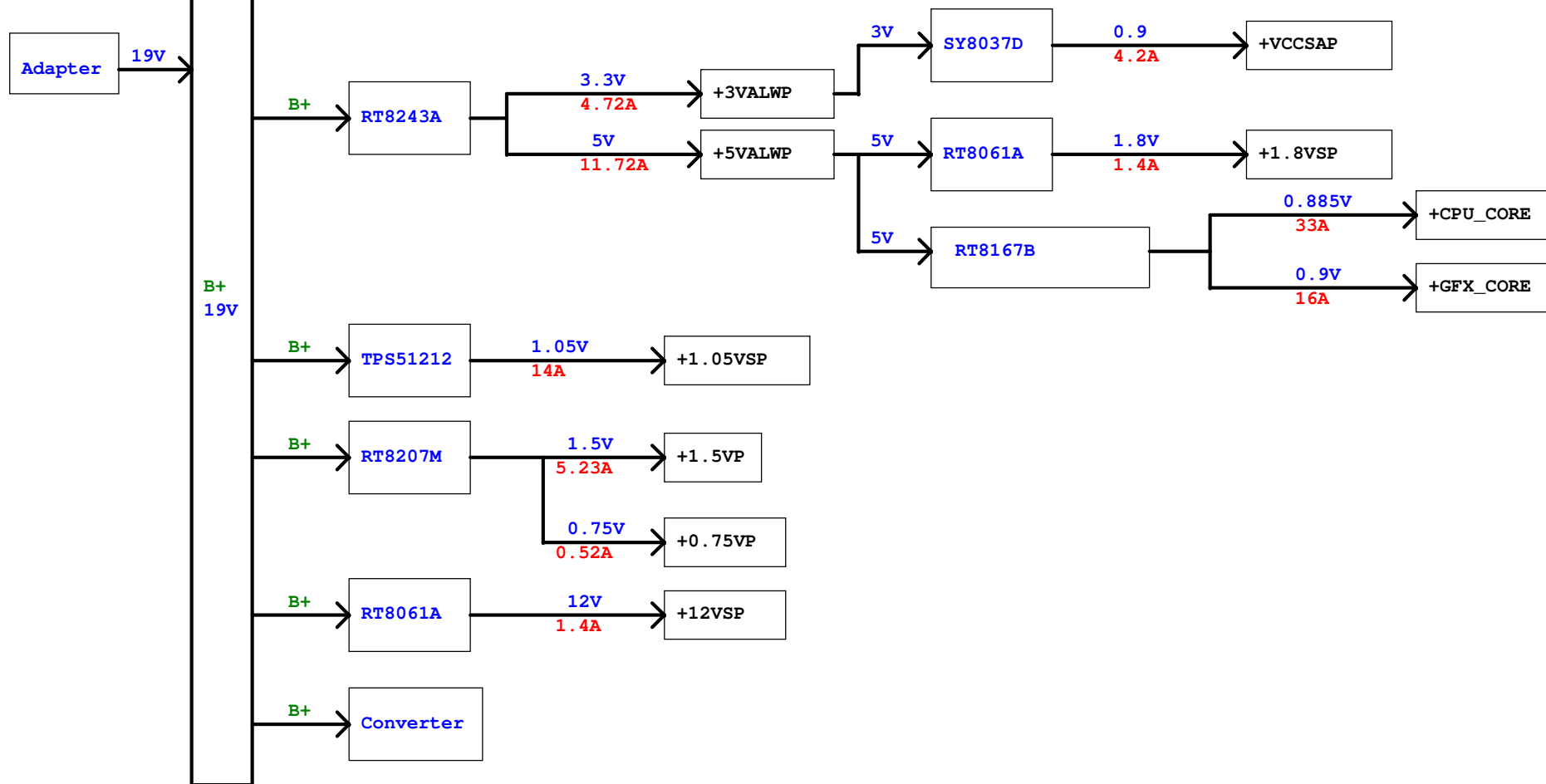
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Version Change List ( P. I. R. List )for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
P38		2012/06/27		PR3=51k	
P38		2012/07/09		PR4=13K , PR6 =20K	Modify feedback Res
P37		2012/07/19		change JDCN1 PN	
P43		2012/07/20		PR53=620k, PR54=44.2k	
P43		2012/07/26		PR53=14k, PR54=1k, add PR55=60.4k	
P37		2012/07/30		PC8=0.022U	
P44		2012/08/06		PR222=13K, PC209=330P, PR255=9.31K	
P40		2012/08/06		PR30,PR43,PR44,PR51,PR204,PR205,PR235,PR236,PR238,PR240,PR241,PR262,PR265,PR266,PR654,PR657 (共16顆換成short pad)	
P44		2012/08/08		PR216=0ohm, PR249=0ohm	
P44		2012/08/08		PR242=51K	

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				Size	Document Number	Rev 0.2
				Date: Friday, August 10, 2012		
				Sheet	47	of 48

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		ME request	0.1	PG#29	Change JHDD1/JODD1 from SP011205226 to SP011207176	7/27	PP
2		Thermal request	0.1	PG#32	Add JP1/JP2 for PCH heat sink	7/27	PP
3	+LAN_VDD_3V3 leakage	HW Design	0.1	PG#31	Change R57.1 from +3VALW to +LAN_VDD_3V3	8/03	PP
4		EMI request	0.1	PG#26	Change L15 from SM070001R00 to SM070002Y00	8/06	PP
5		Vender suggest	0.1	PG#30	Change Y13 from SJ10000DJ00 to SJ10000E800	8/06	PP
6		Vender suggest	0.1	PG#30	Change C2794/C2795 from 27pF to 12pF	8/06	PP
7	Board ID update	HW Design	0.1	PG#35	Change R2676 from 0 ohm to 8.2K ohm	8/07	PP
8		EMI request	0.1	PG#17	Delete T223,T224,T248	8/08	PP
9		EMI request	0.1	PG#14	Delete T215,T216	8/08	PP
10		ESD request	0.1	PG#5	Add C105 180pF CAP	8/08	PP
11		ESD request	0.1	PG#18	Add C106 180pF CAP	8/08	PP
12		ESD request	0.1	PG#17	Add C107 180pF CAP	8/08	PP
13	LAN ON/OFF function	BIOS request	0.1	PG#30 PG#35	Add R2835 and EC_PHY_OFF# to EC GPIO40(Pin73)	8/08	PP
14		Vender suggest	0.1	PG#27	Change U97 from SA000001N000 to SA000005N000	8/08	PP
15		HW Design	0.1	PG#23 PG#34	Change U46,U96 from SA000039E00 to SA00003DR00	8/08	PP
16		HW Design	0.1	PG#35	DEL T16,T17,T23,T24,T25,T26,T27,T28	8/09	PP
17		HW Design	0.1	PG#35	Add C108,C109 as DFB request	8/09	PP
18		HW Design	0.1		Change R2891,R2893,R2788,R2802,R2803,R2804,R2805,R2806 ,R2808,R2809,R2810,R2811,R2814,R2815,R2816,R2817 ,R2818,R2819,R2820,R2832,R2685,R2688,R2690,R2691 ,R2694,R2695,R24,R26,R27,R57,R2222,R775,R777,R778, R779,R39,R40,R42,R43,R2951,R2953,R2954,R2956,R2962, R2966,R13,R23,R2874,R2790,R2791,R111,R112 from 0_ohm to 0_ohm_short	8/09	PP
19		HW Design	0.1	PG#35	Add C108,C109 as DFB request	8/09	PP
20	For S5 power consumption reduce	HW Design	0.1	PG#35	Change +VCCSUS3_3 SMT BOM	8/09	PP
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